Narrative Description

Part 2 : Figures

MUCOLEX II

LINK ENCRYPTION EQUIPMENT TYPE UA8244

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Nato Confidential

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LIST OF EFFECTIVE PAGES

The following list shows the page number and revision status of every page in part 2 of this document.

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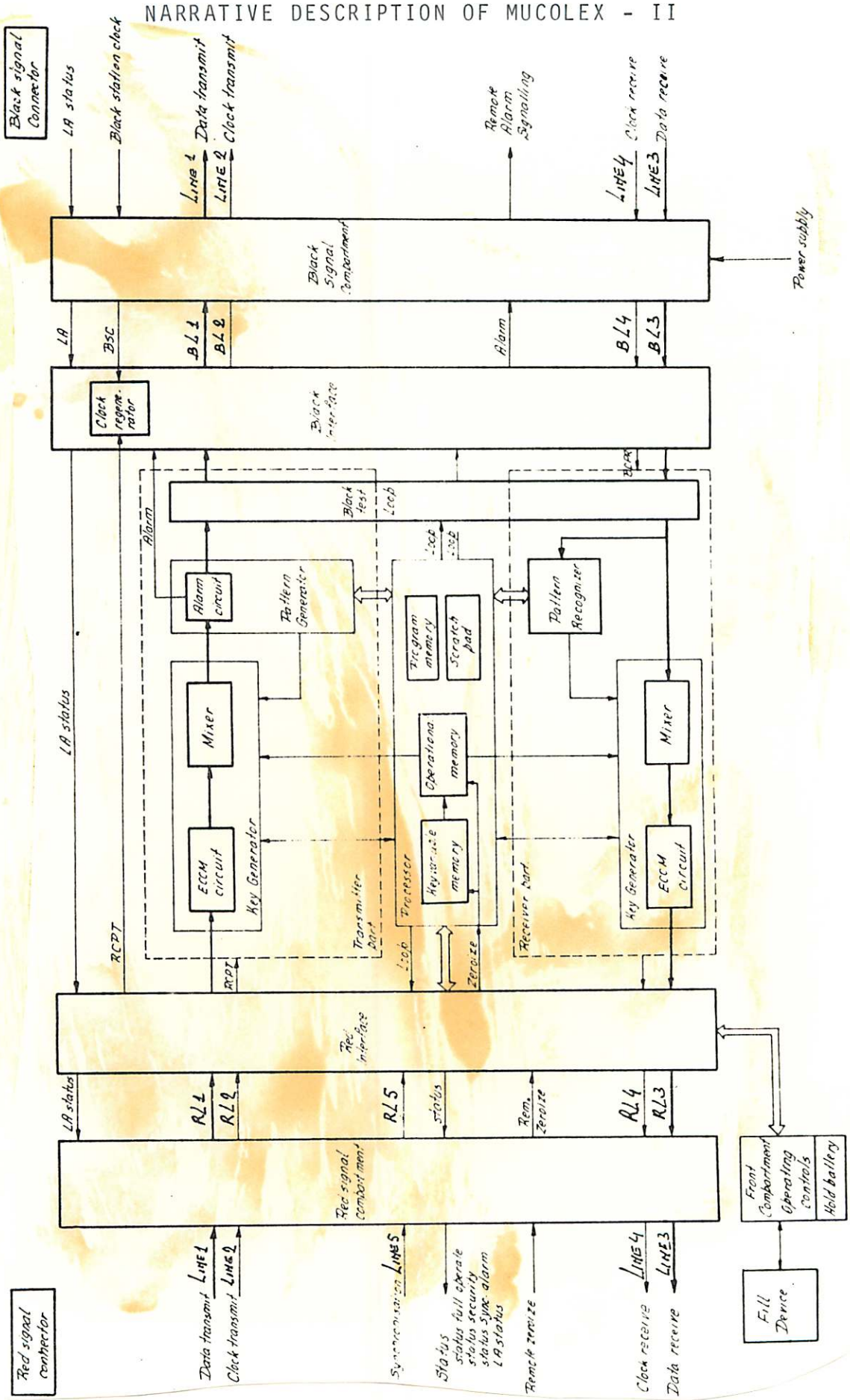

Figure 1-1: Block diagram, Mucolex II Link Encryption Equipment

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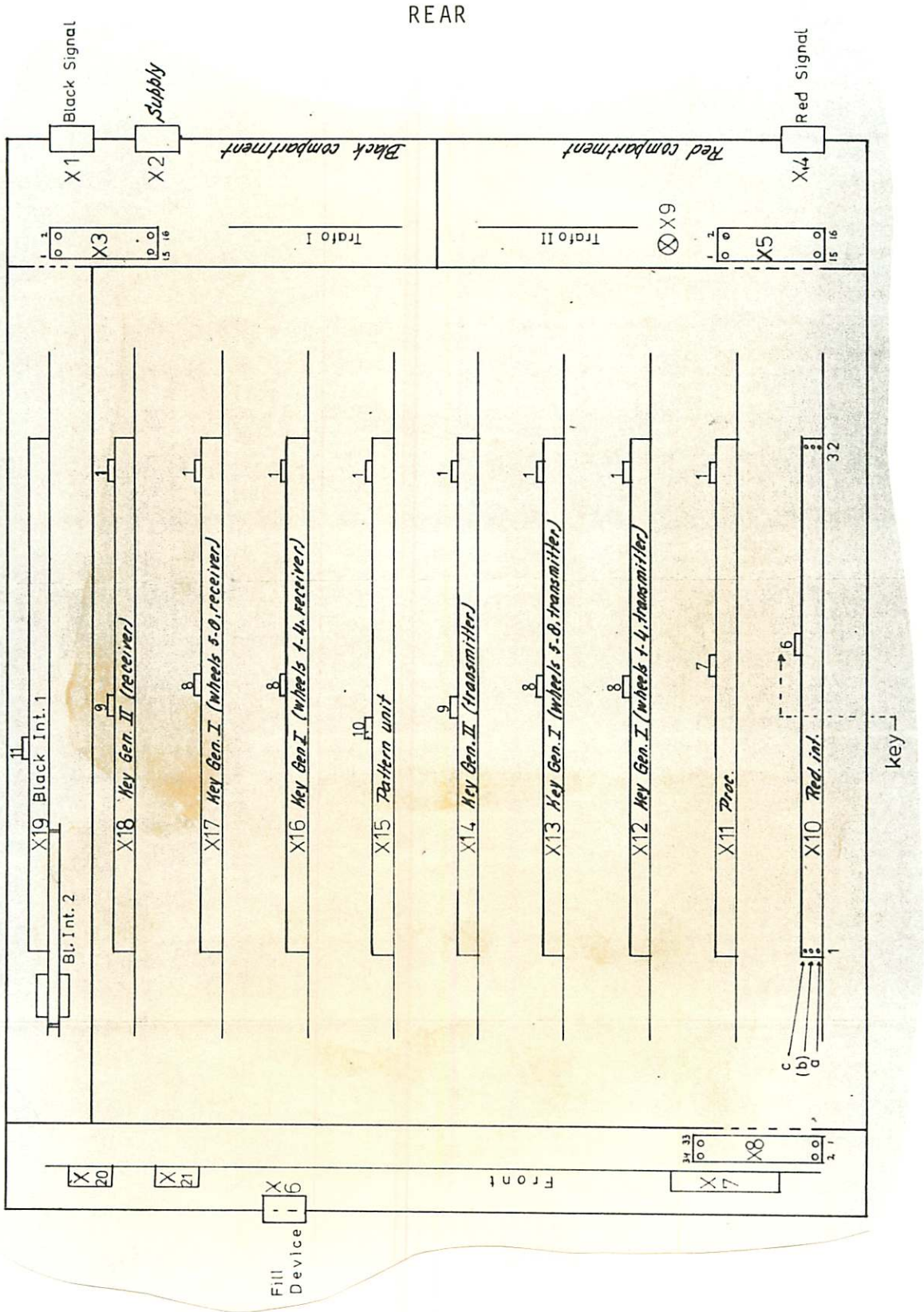
NARRATIVE DESCRIPTION OF MUCOLEX - II



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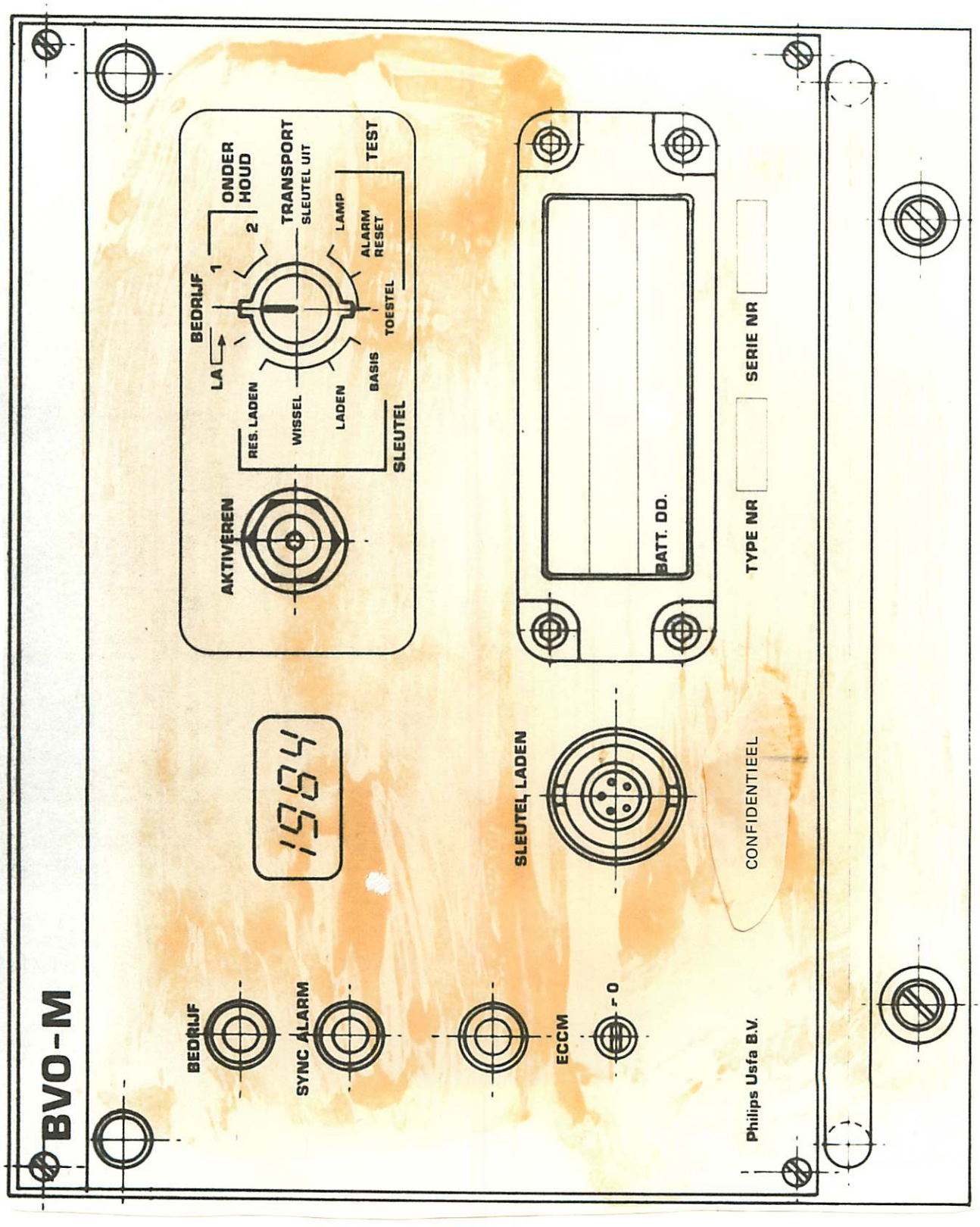

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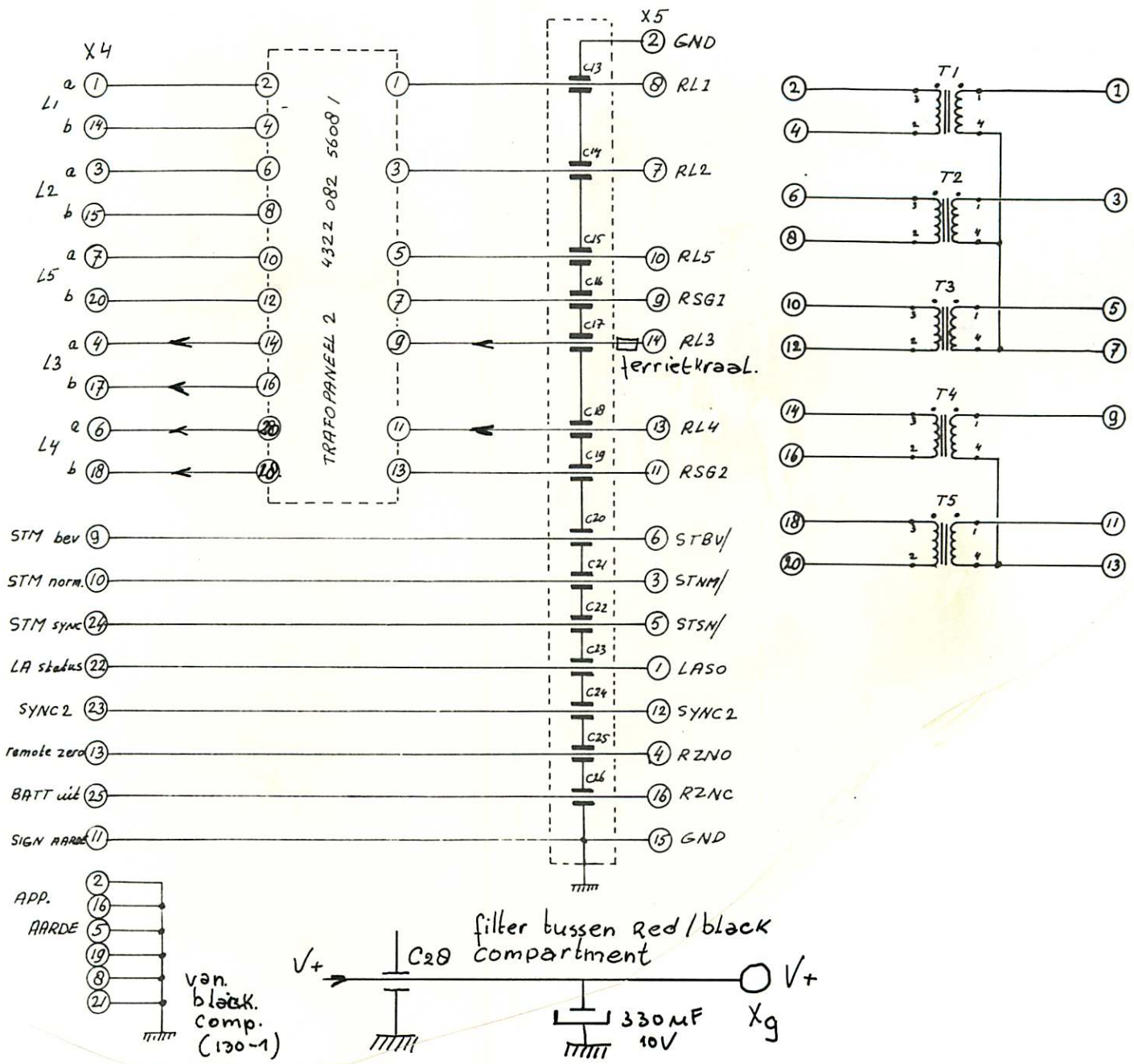


Figure 2.1-1: Red filter compartment.

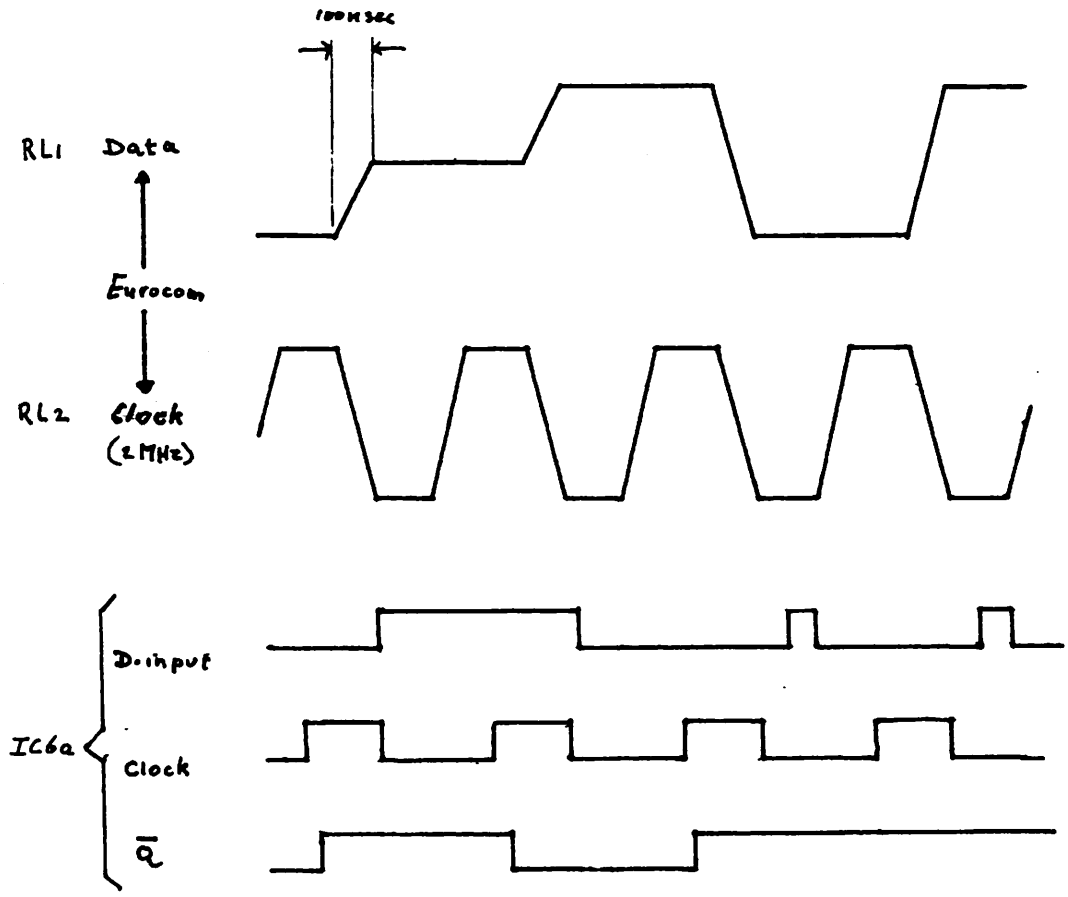
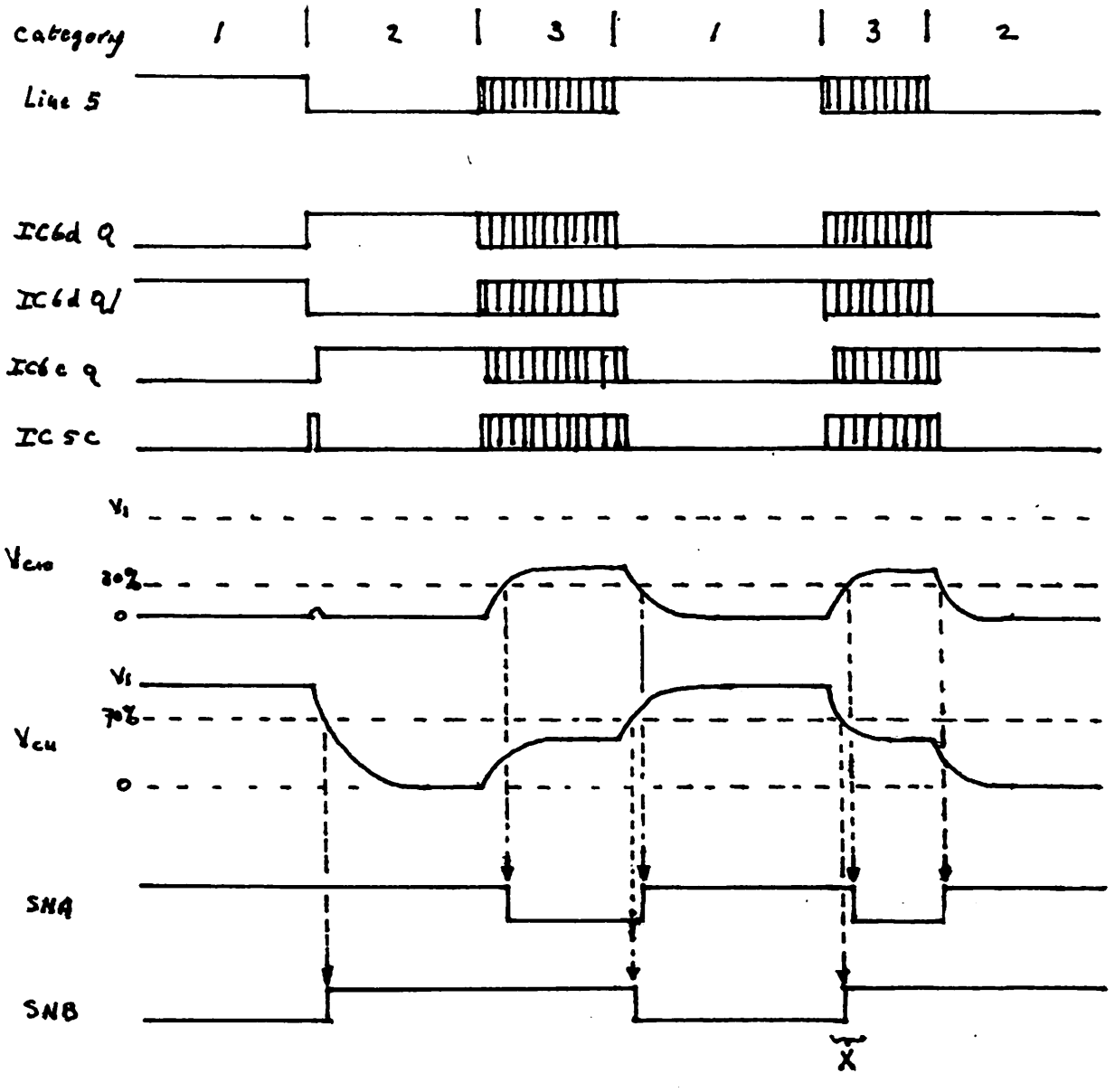


Figure 2.1-2: Pulse diagram, EUROCOM - LSTTL conversion



	SNA	SNB
Category 1	1	0
Category 2	1	1
Category 3	0	1
Transiênt	1	1

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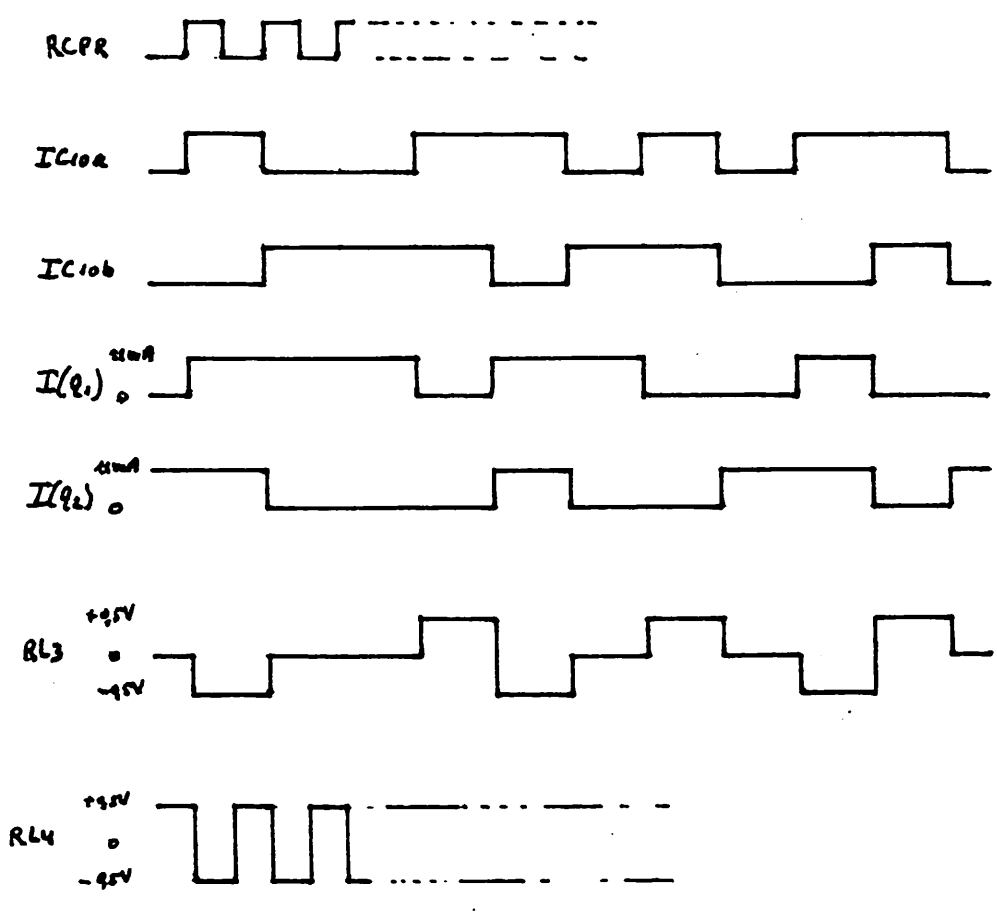
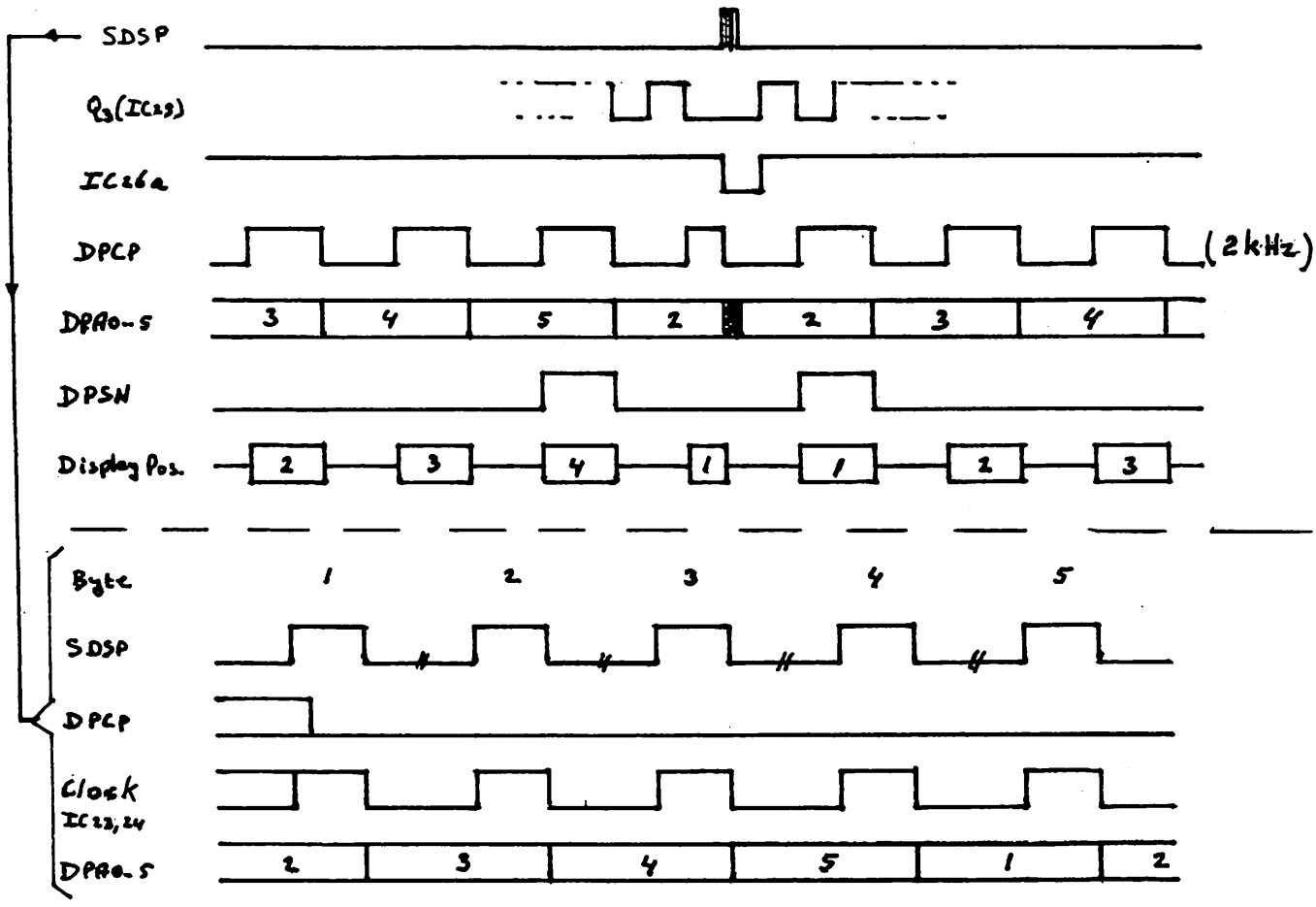


Figure 2.1-4: Pulse diagram, LSTTL - EUROCOM conversion



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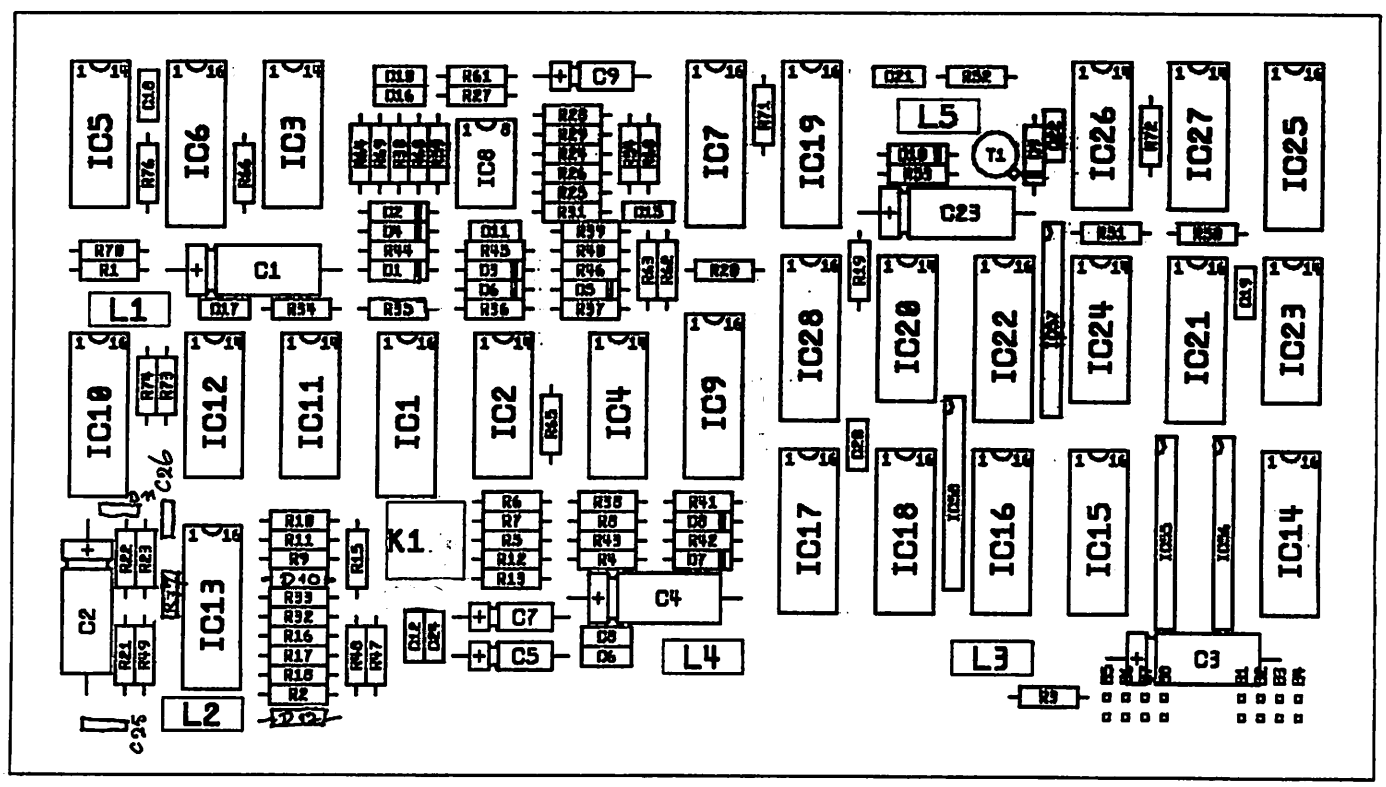
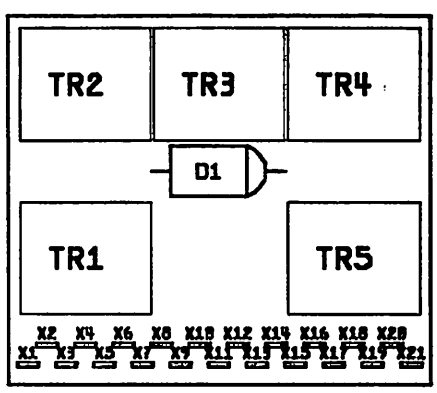


Figure 2.1-9: Red interface panel



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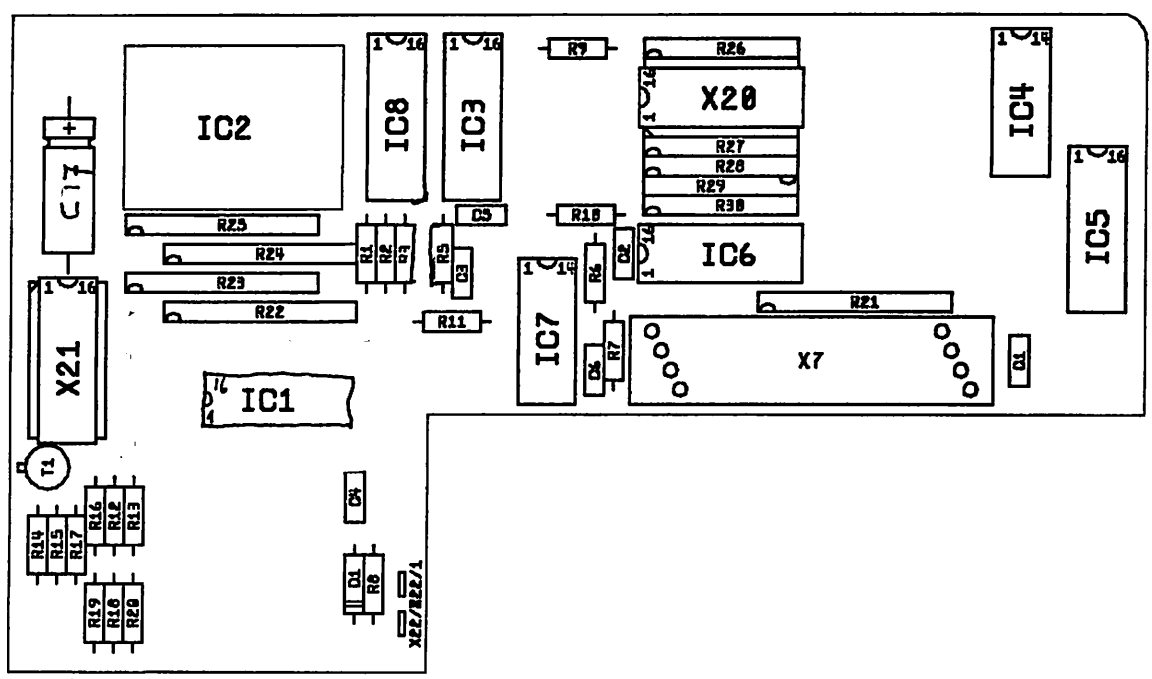

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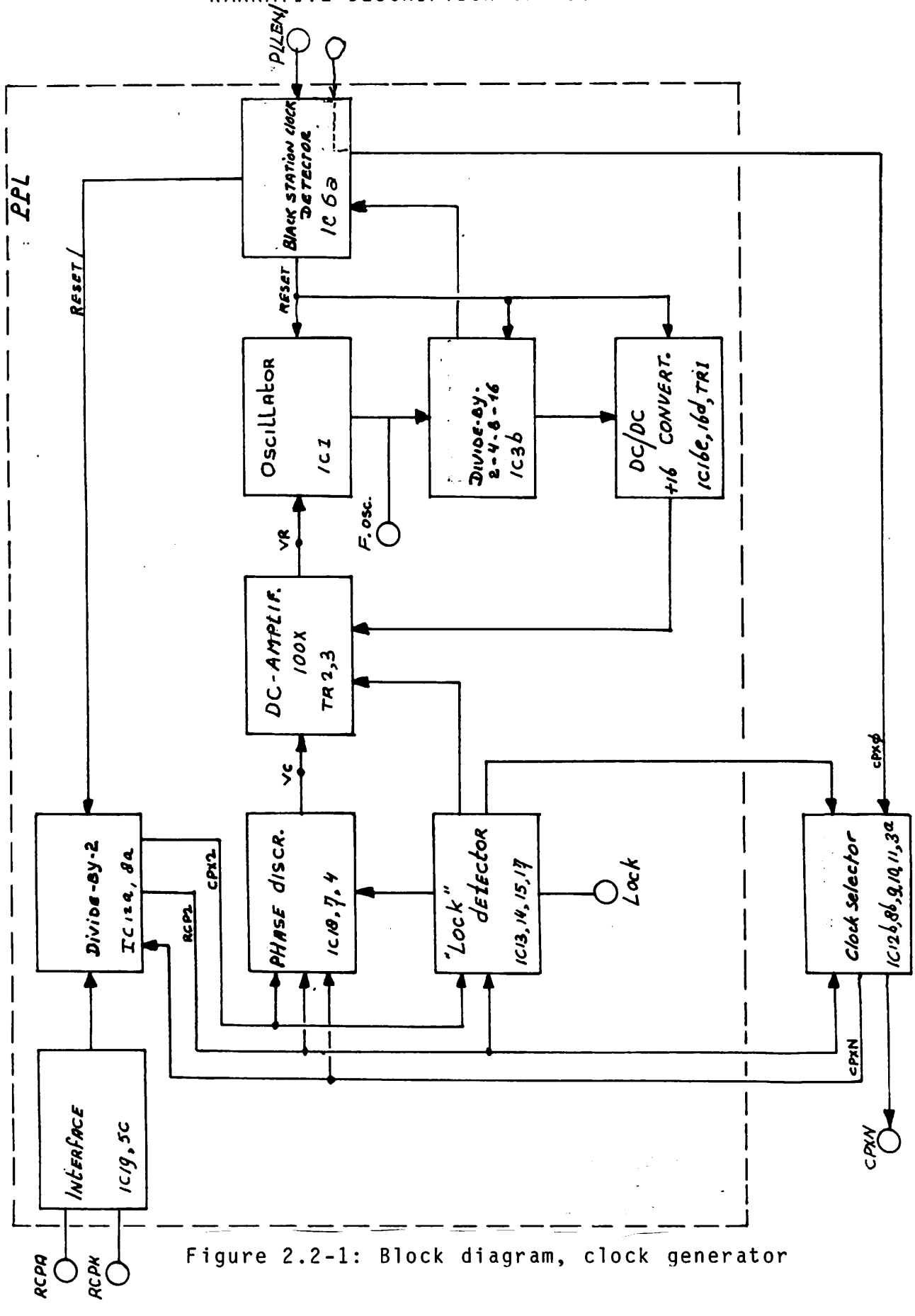
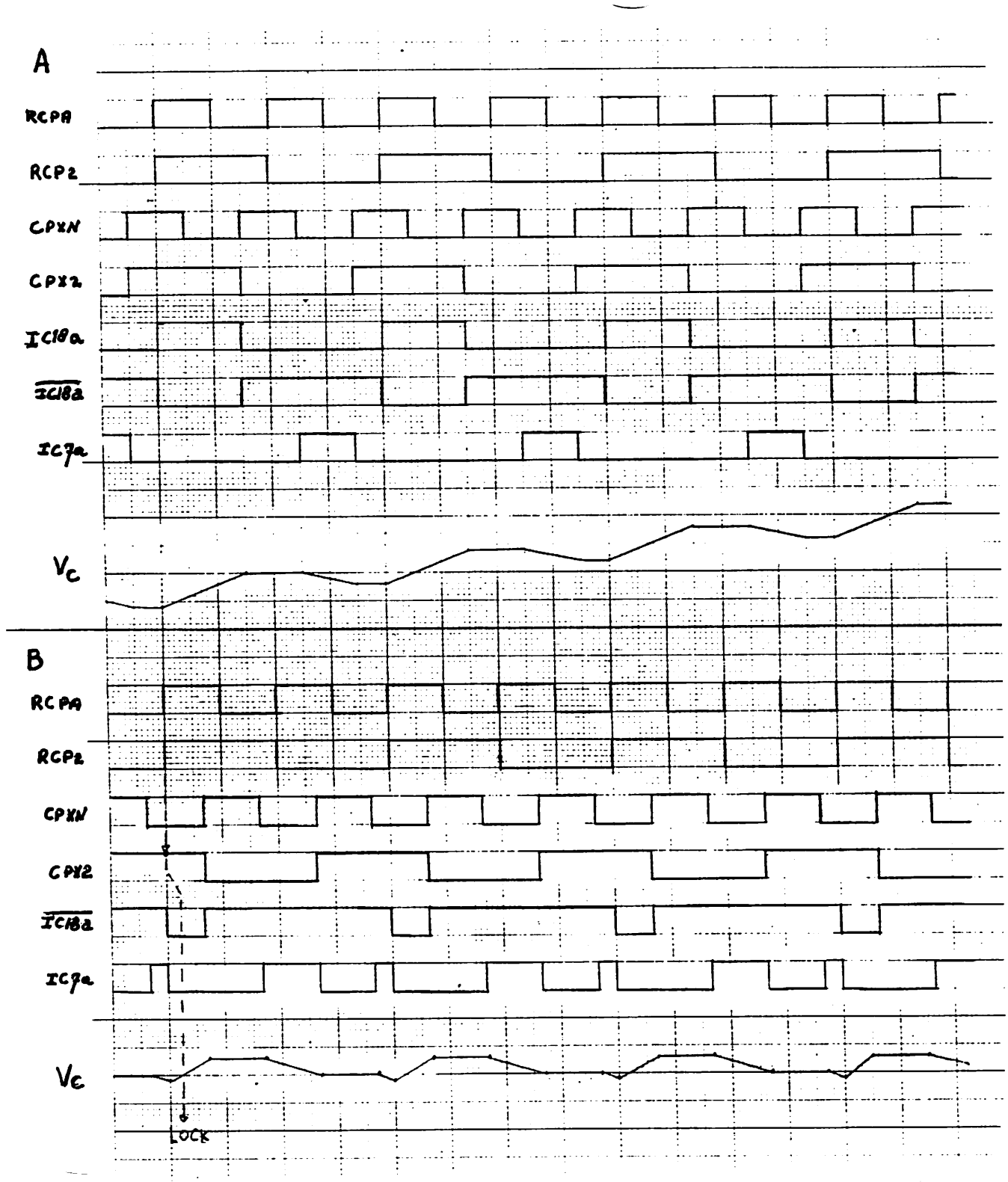


Figure 2.2-1: Block diagram, clock generator



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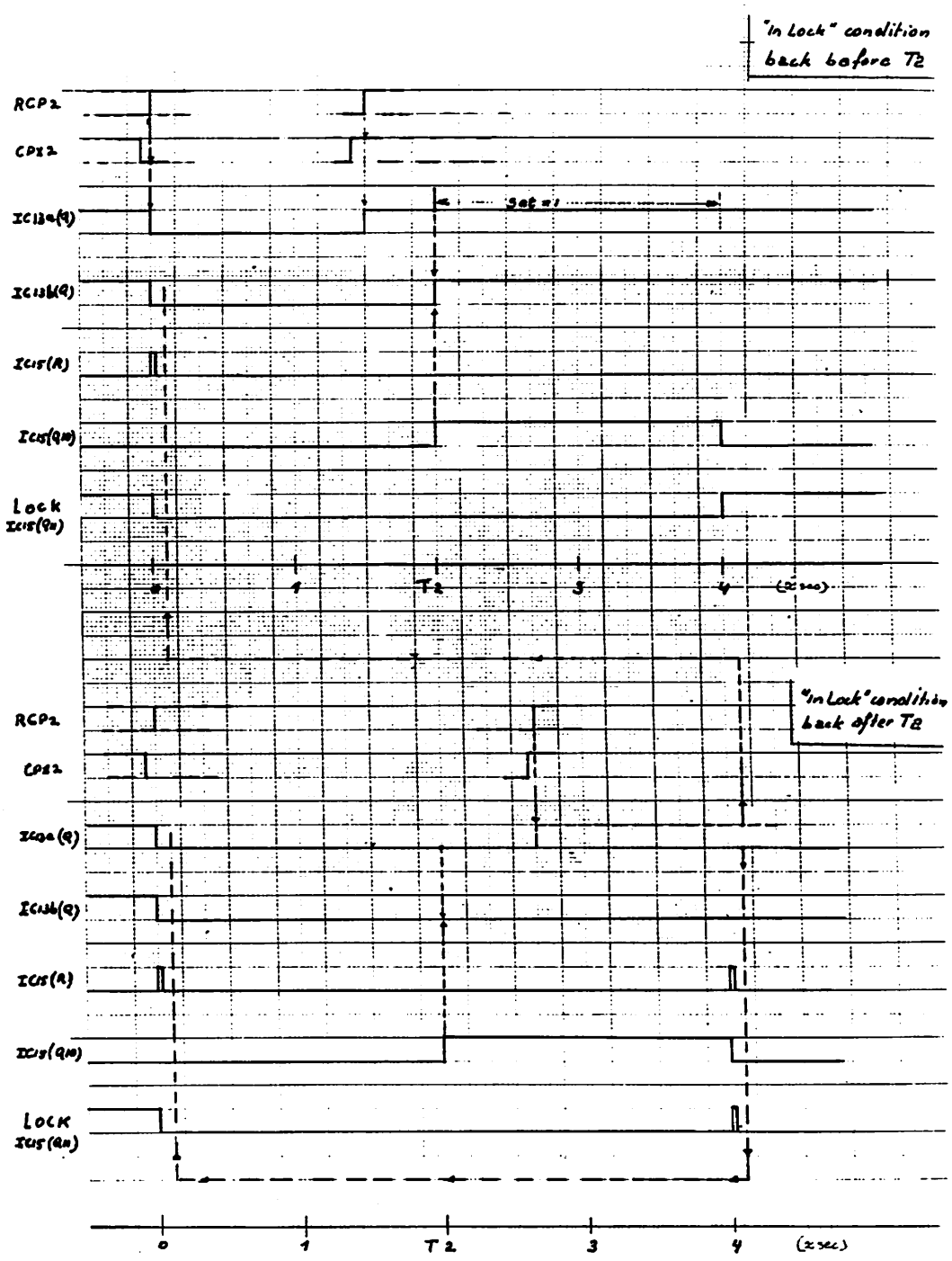

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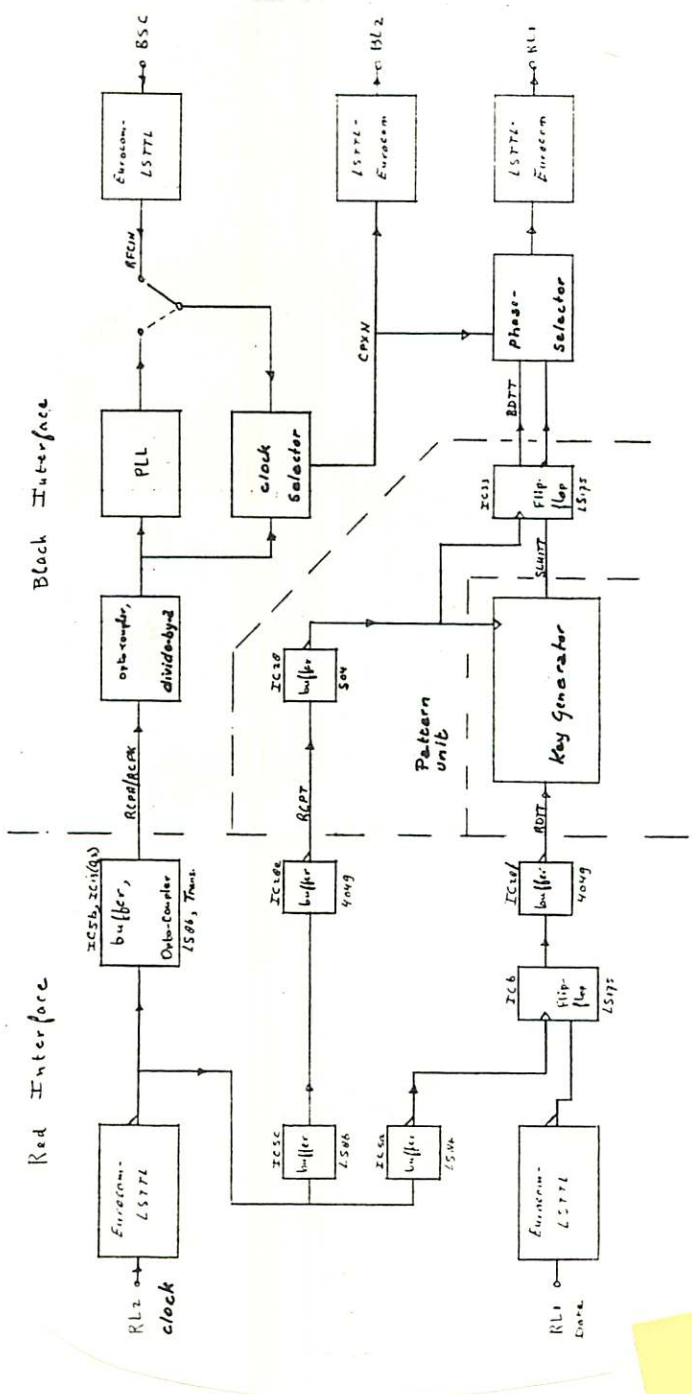

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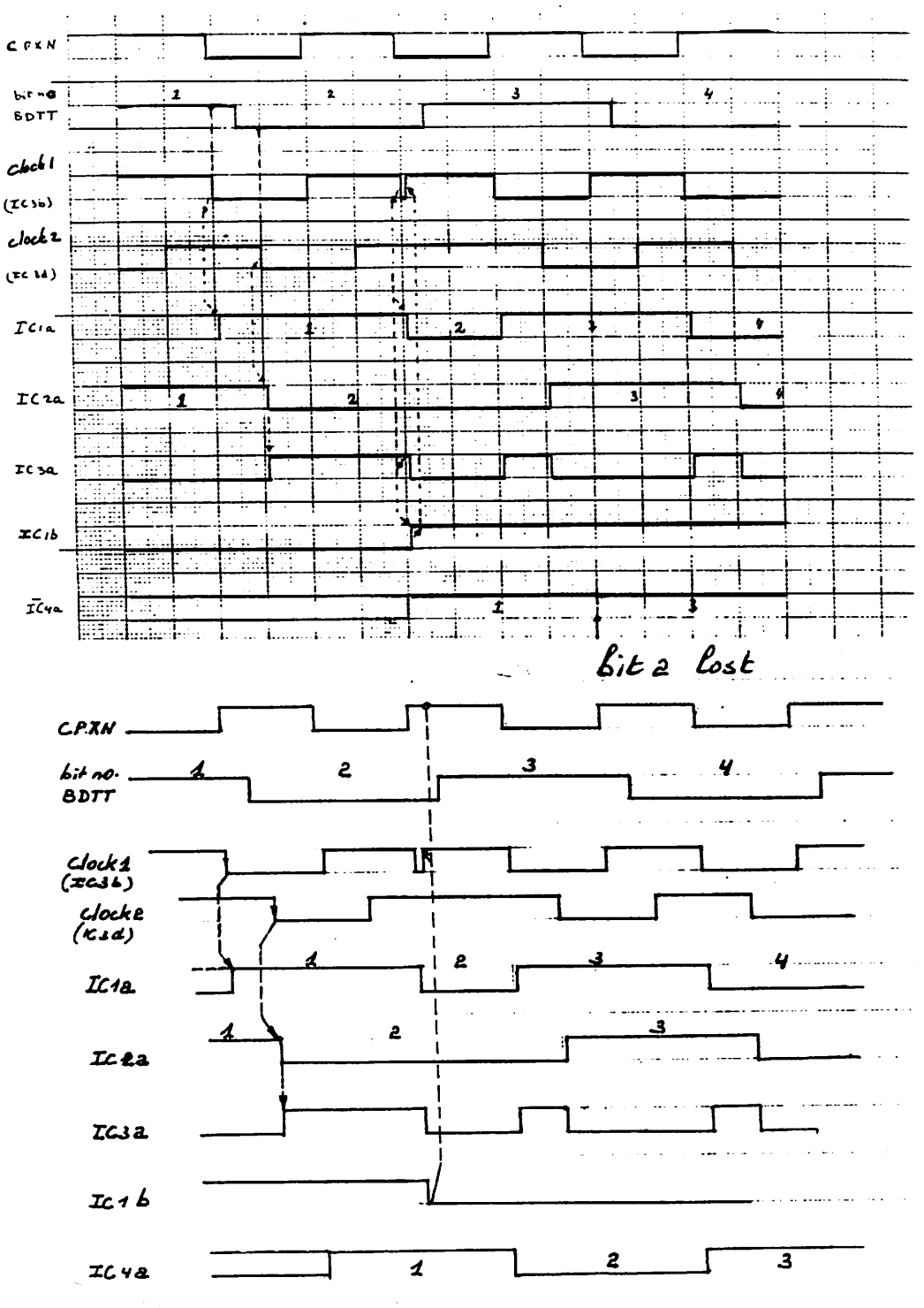

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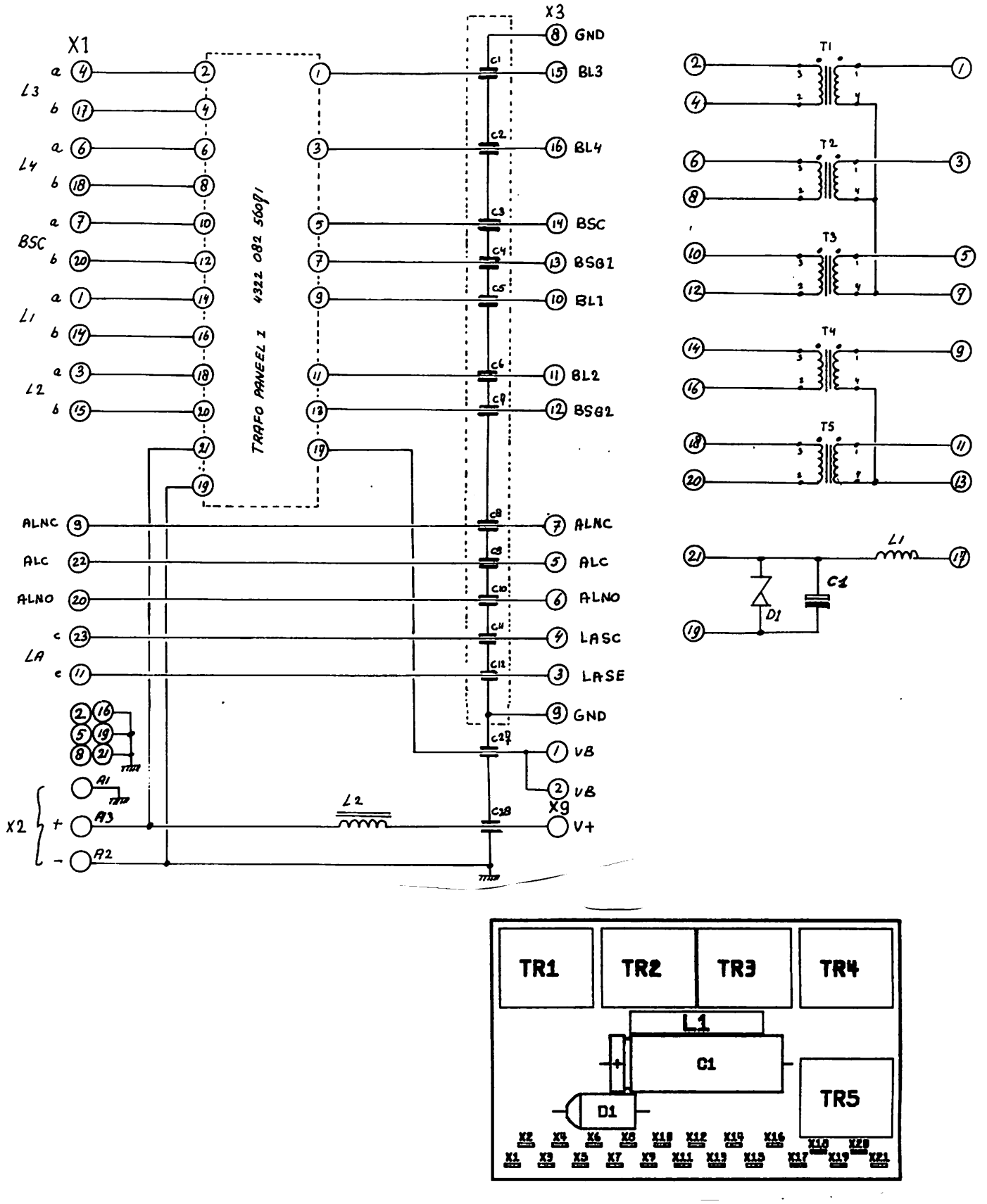

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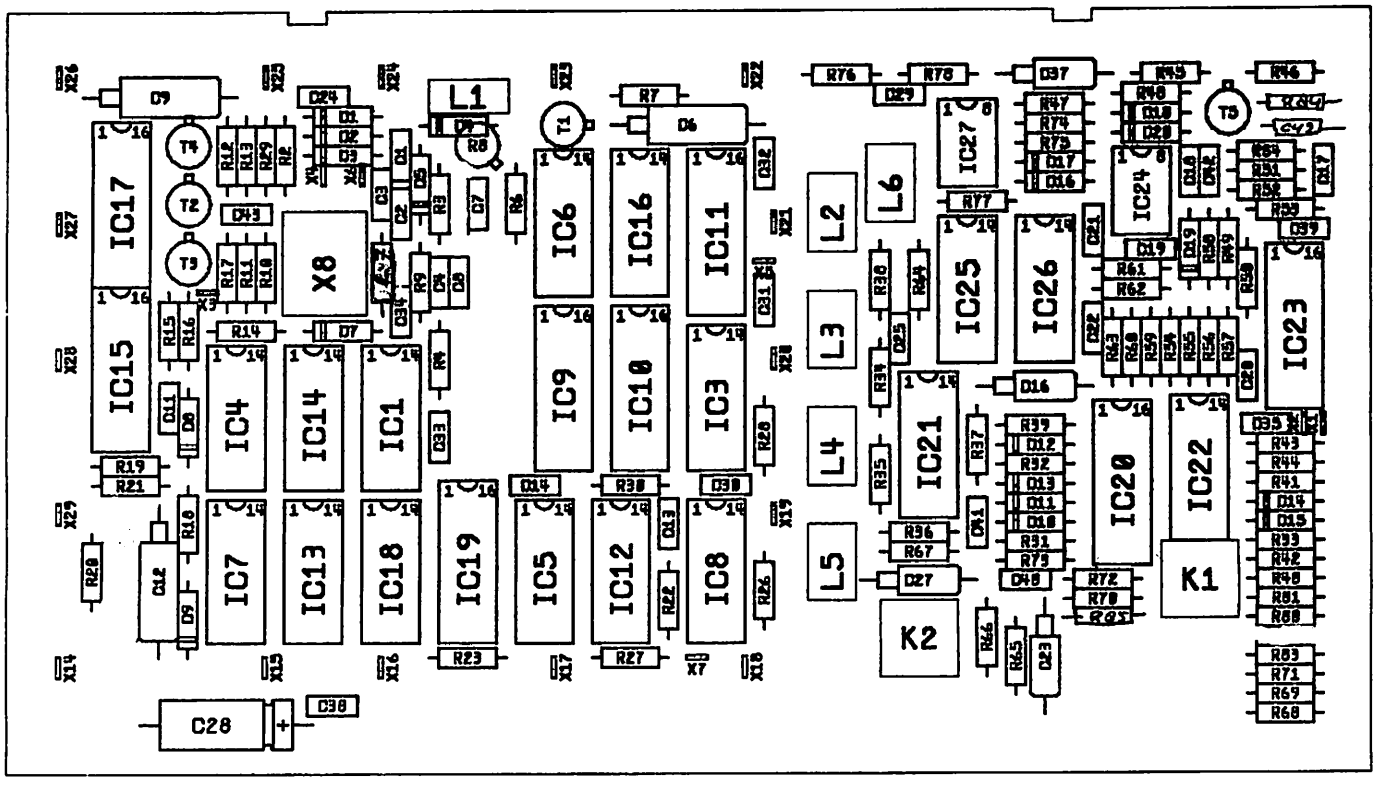

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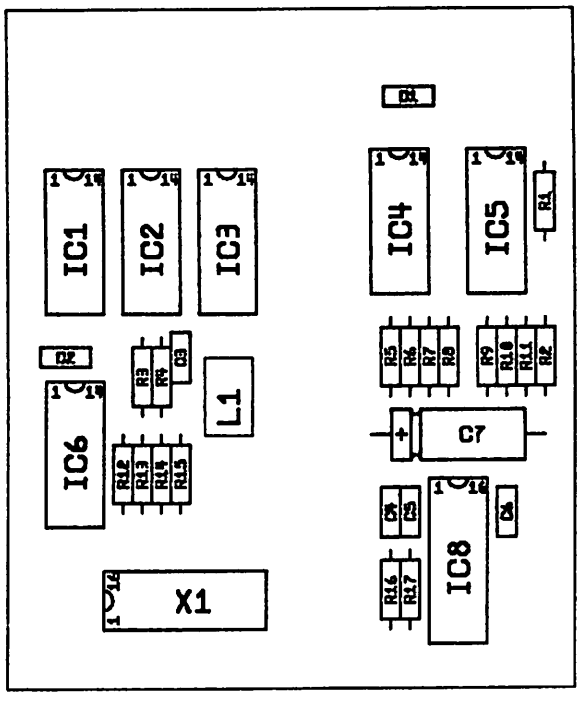

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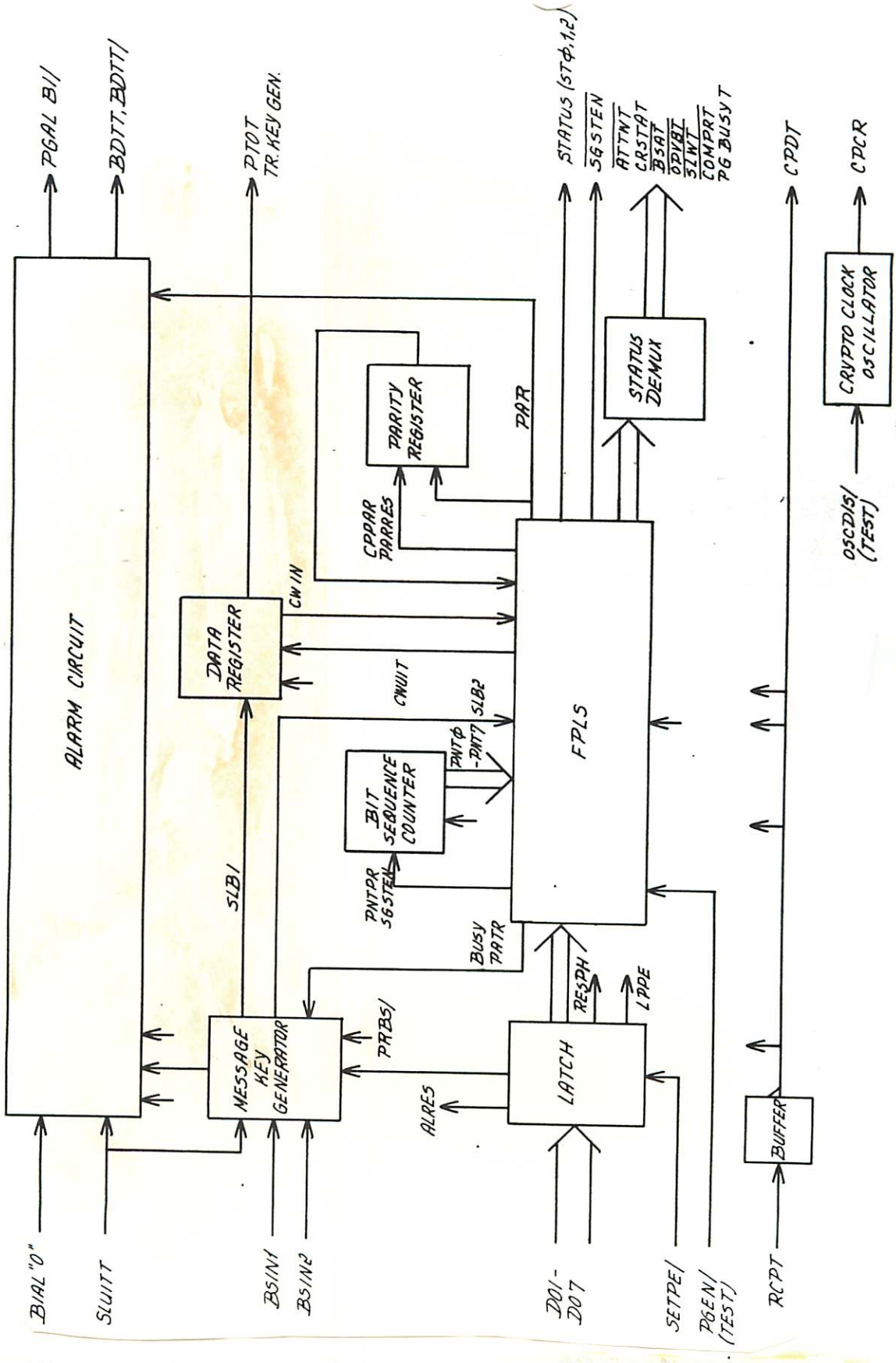

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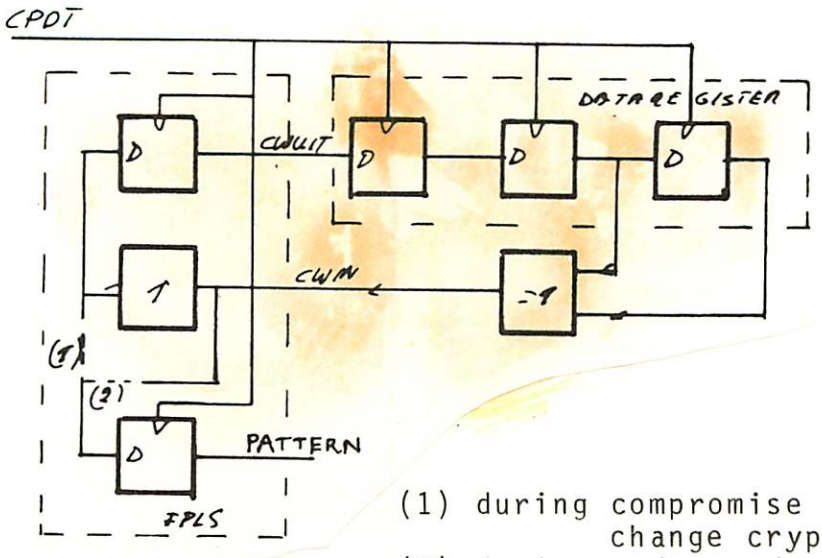

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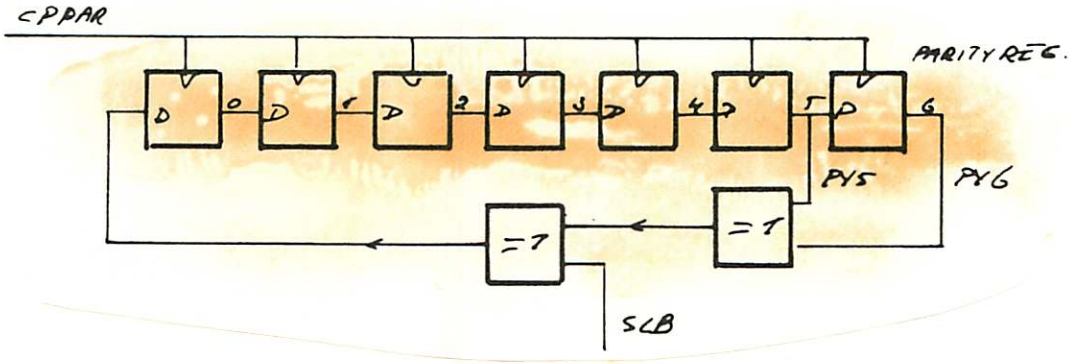

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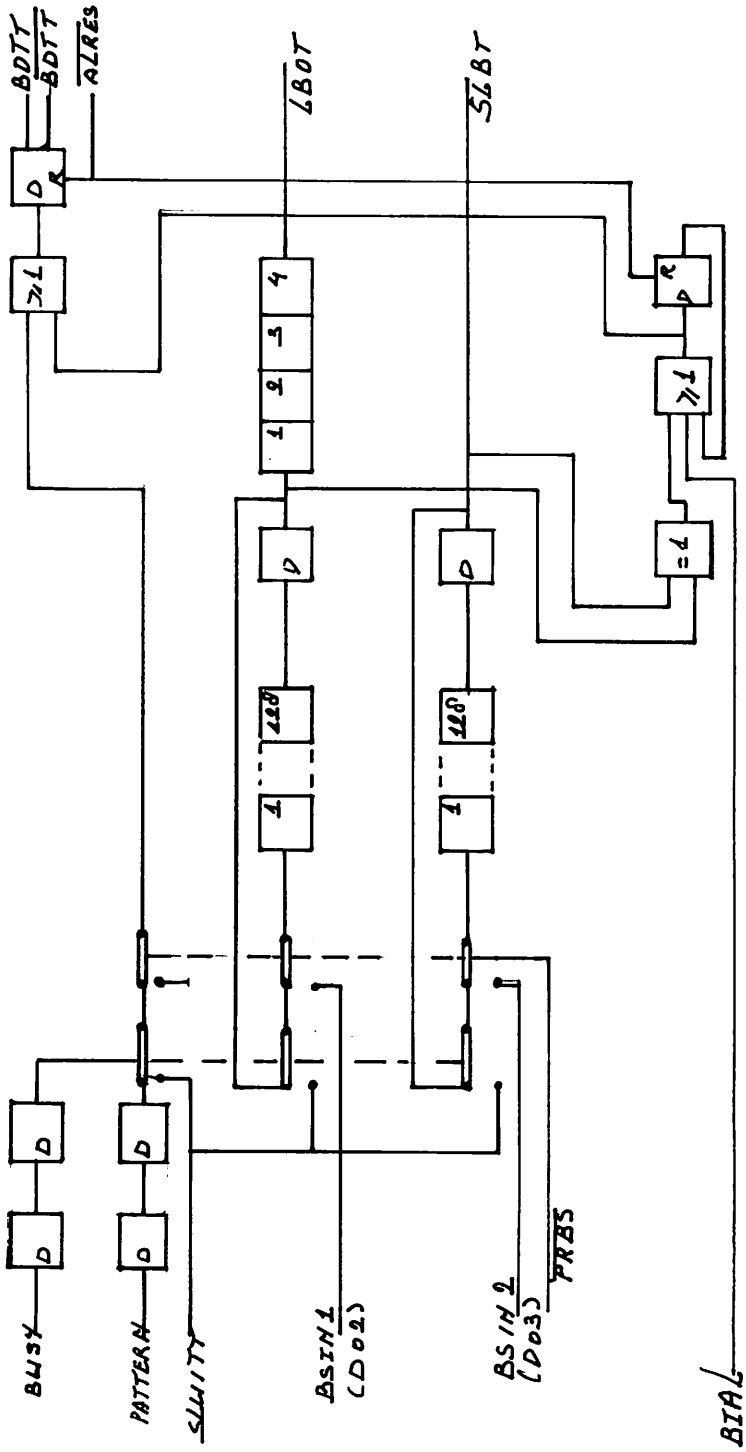


Figure 2.3-4: Diagram message key generator and alarm circuit

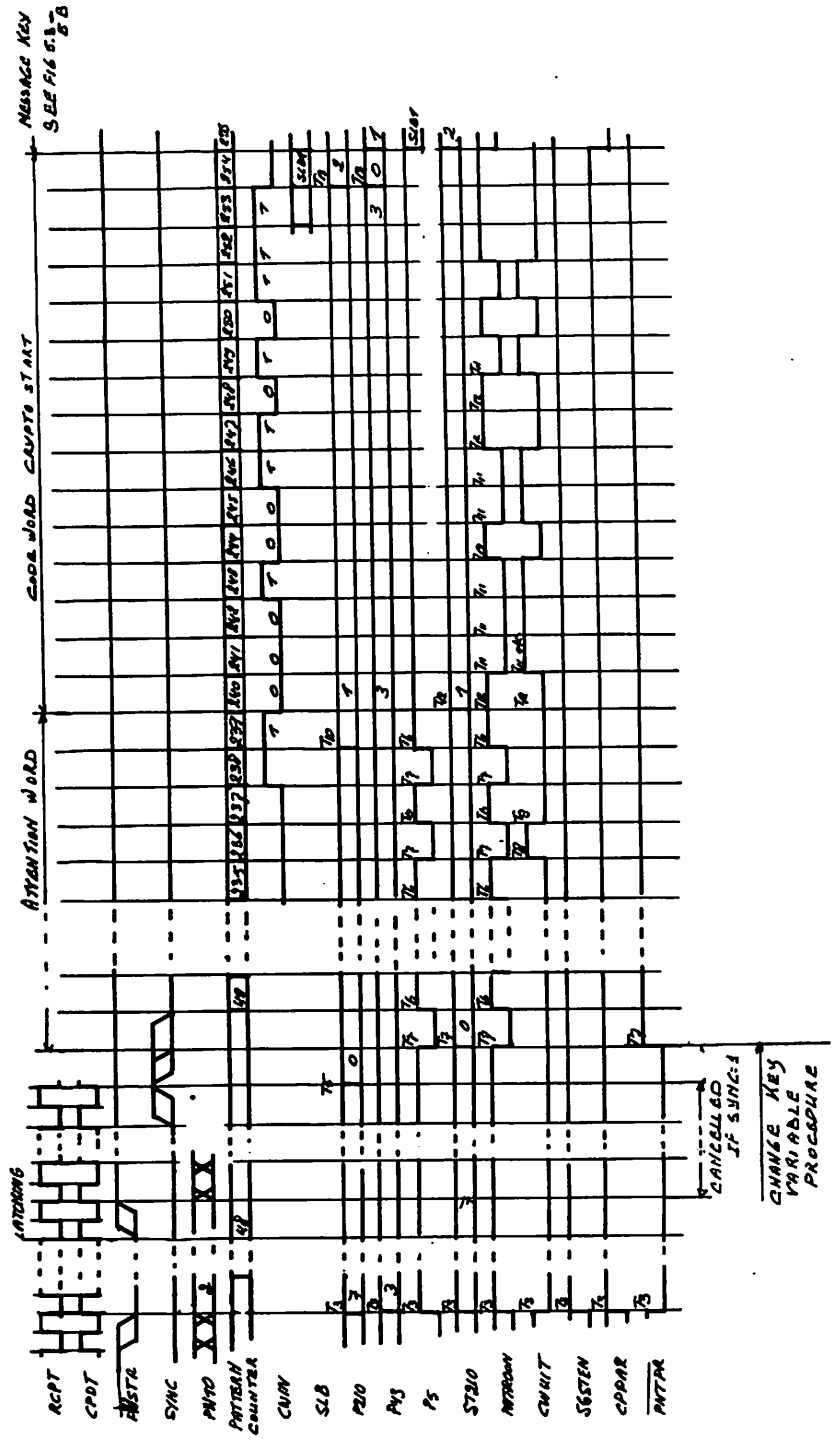


Figure 2.3-5a: Pulse diagram, crypto start procedure

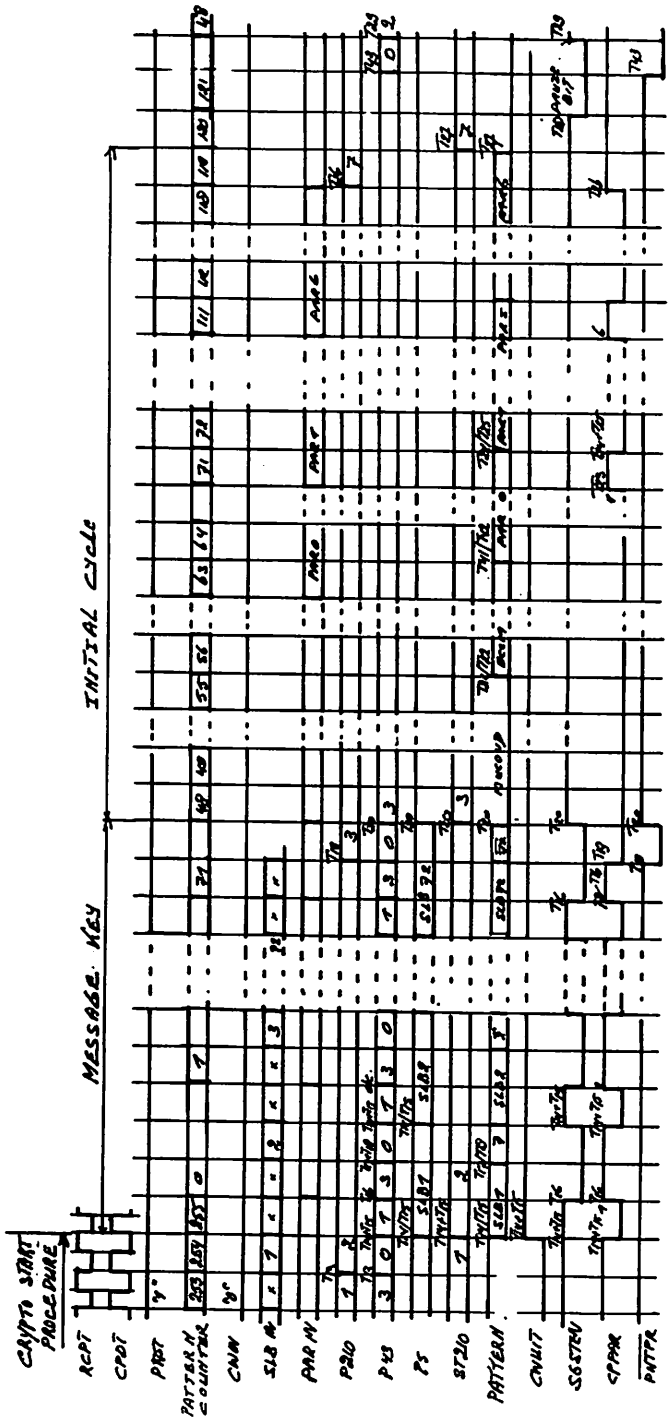


Figure 2.3-5b: Pulse diagram, crypto start procedure (continued)

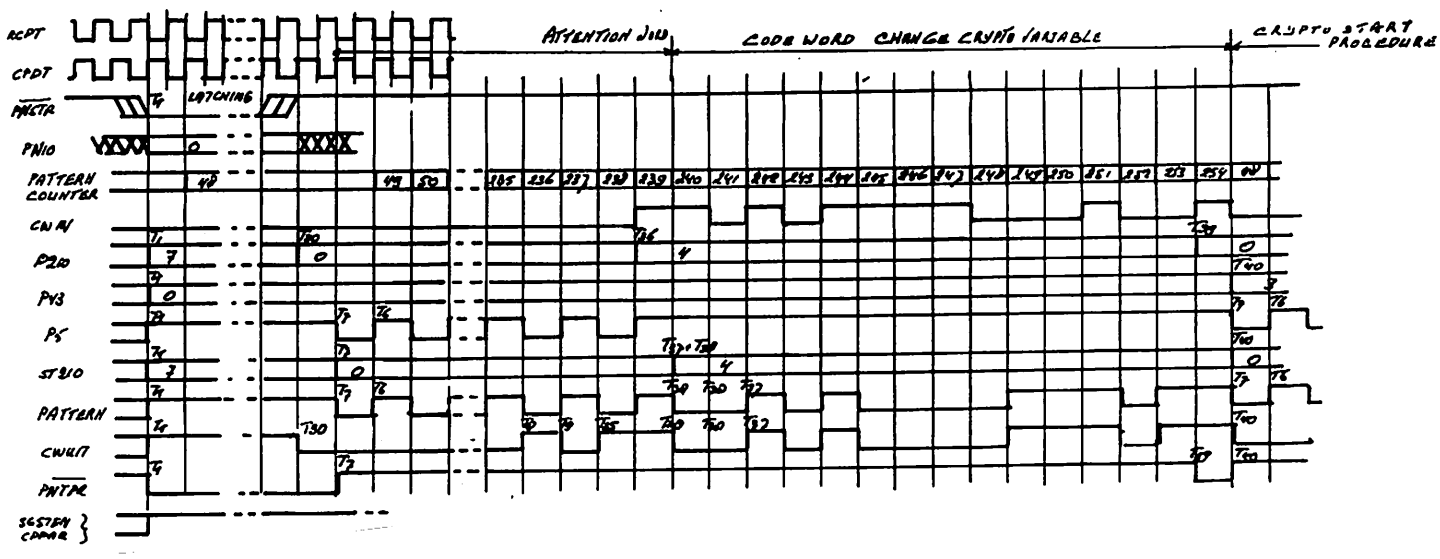
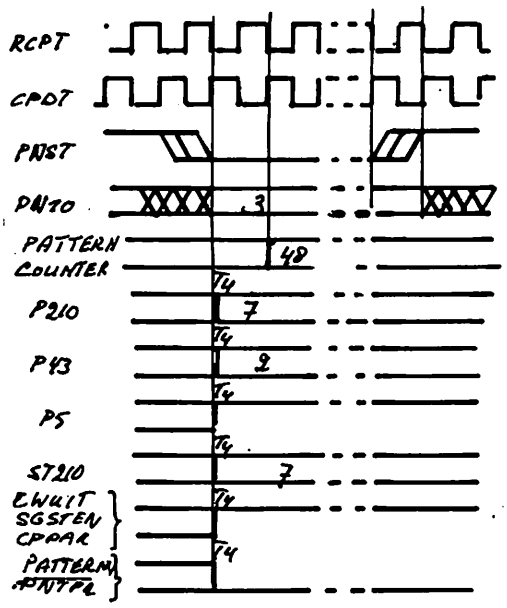


Figure 2.3-6: Pulse diagram, change crypto variable procedure



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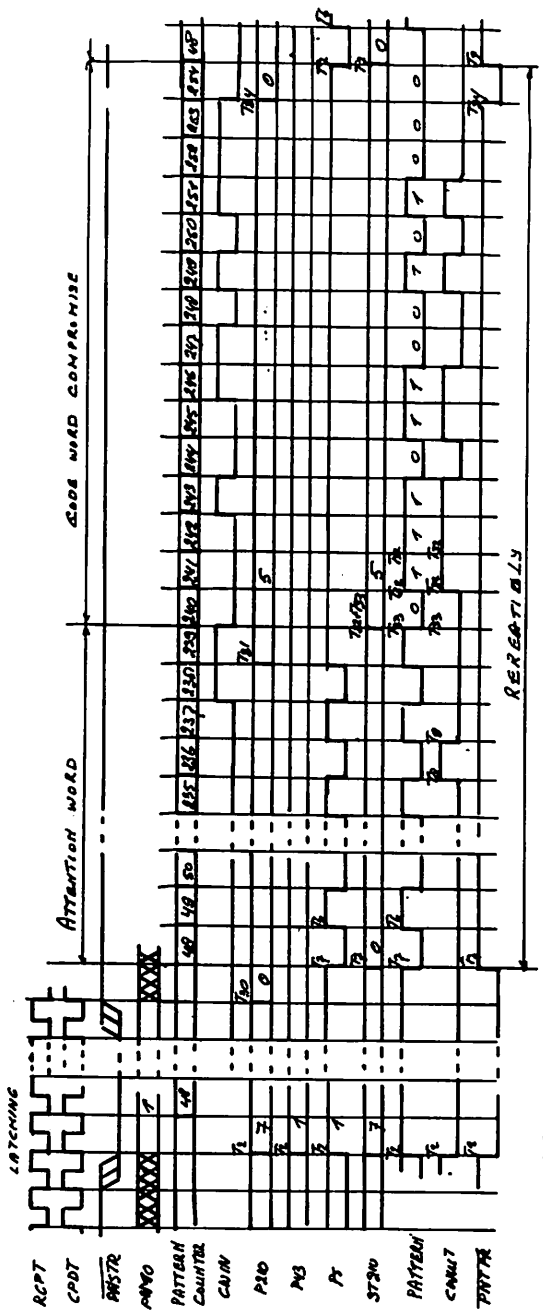


Figure 2.3-7: Pulse diagram, compromise procedure

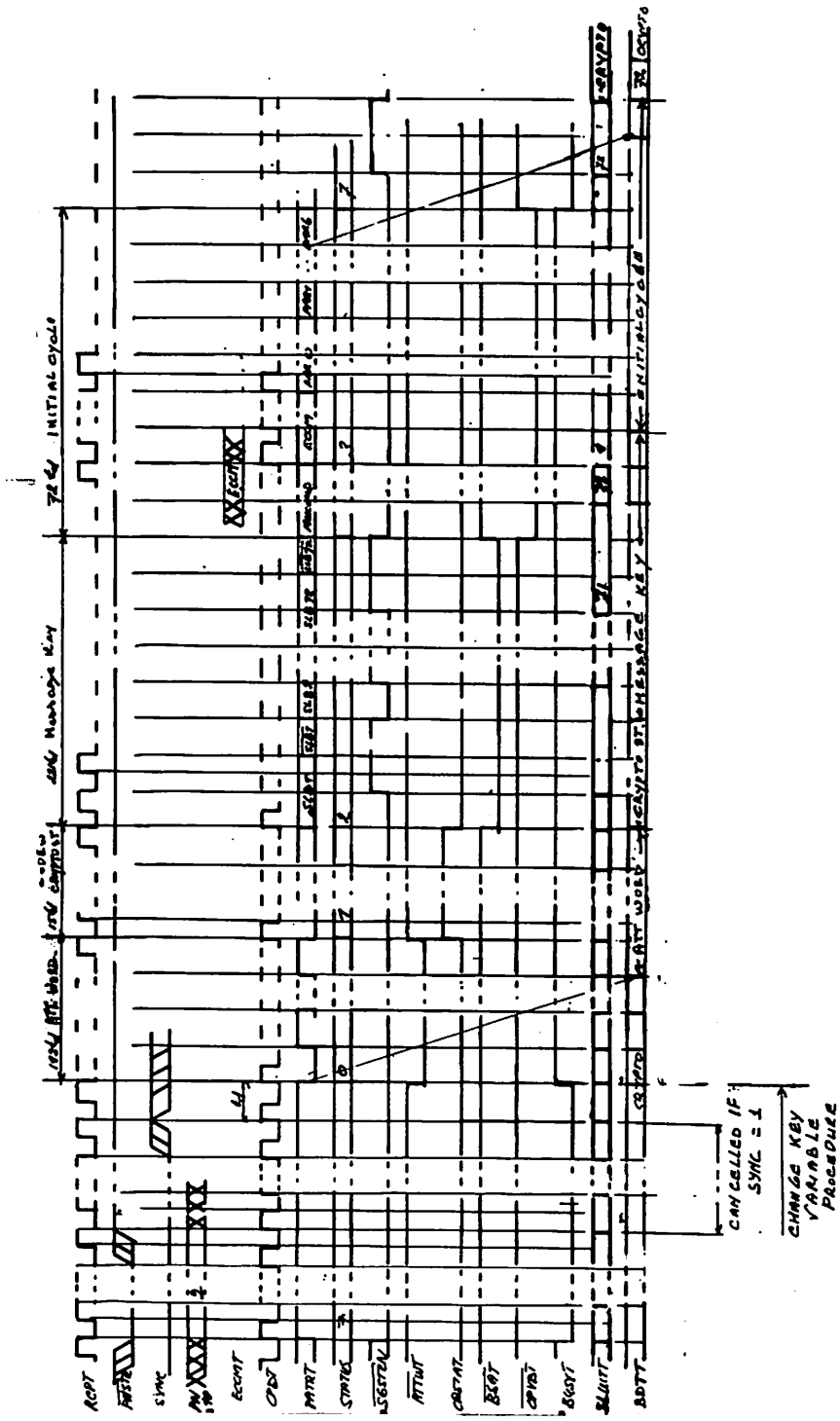


Figure 2.3-9: Pulse diagram, interface signals
crypto start procedure

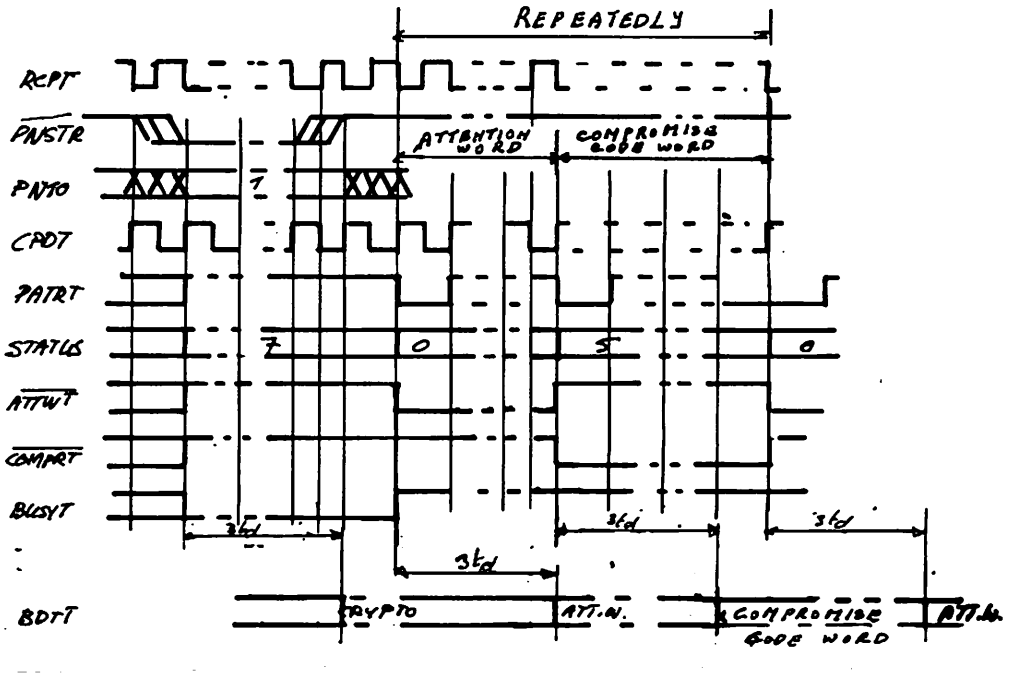


Figure 2.3-10: Pulse diagram interface signals during compromise procedure

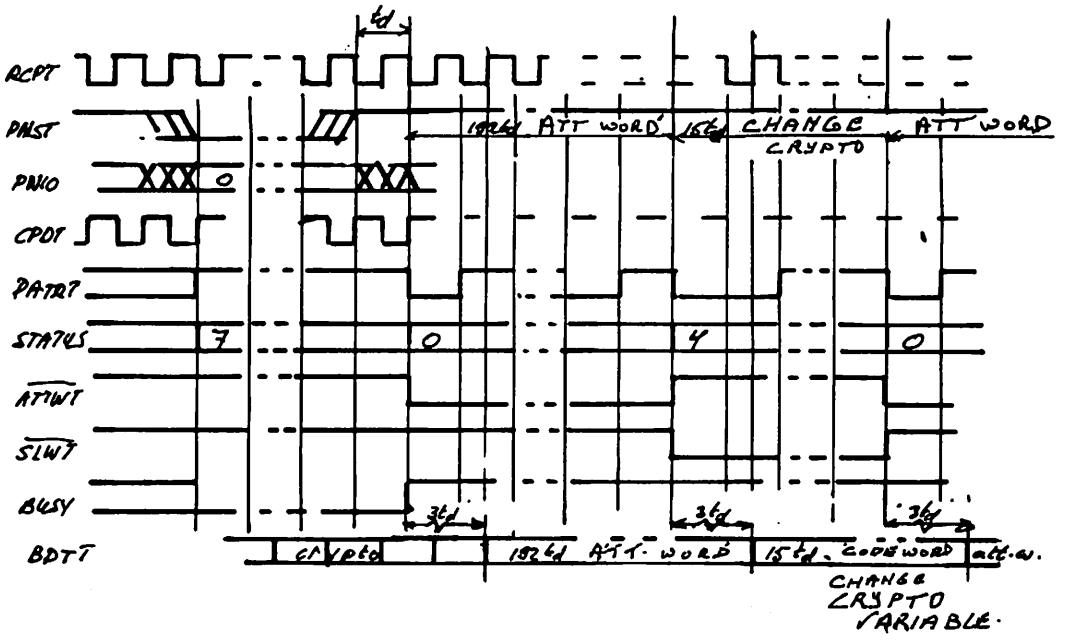


Figure 2.3-11: Pulse diagram, interface signals during change crypto variable procedure

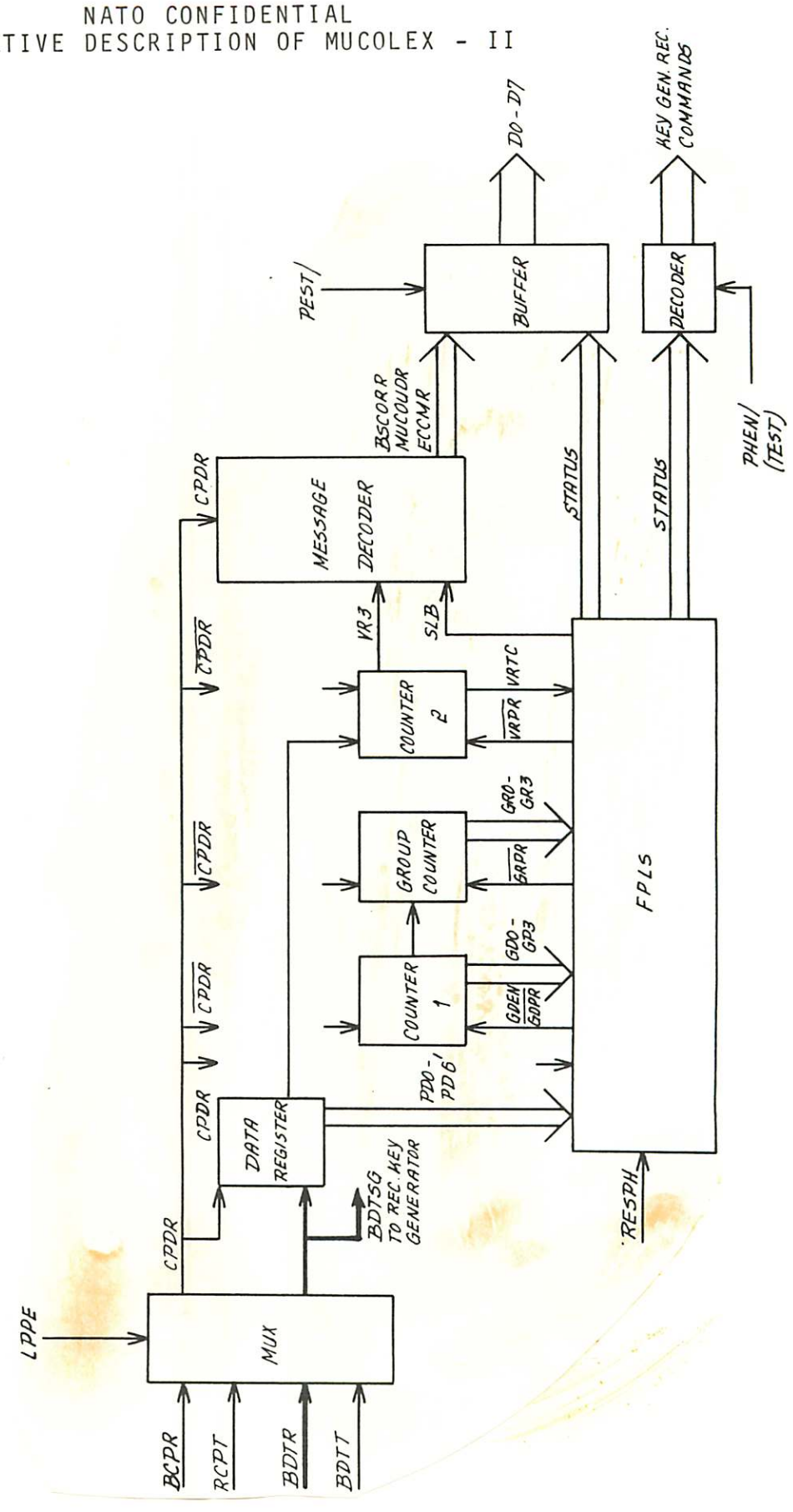


Figure 2.4-1: Block diagram, pattern recognition circuit

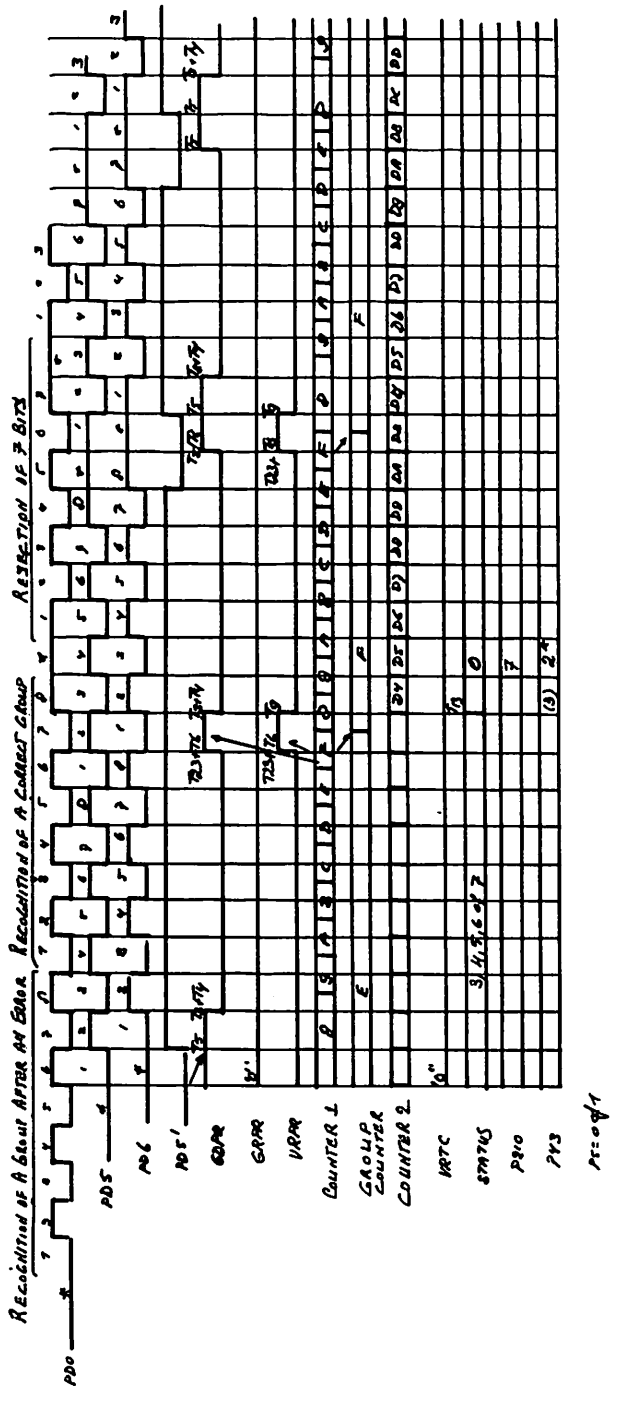


Figure 2.4-2: Pulse diagram, recognition of attention-word

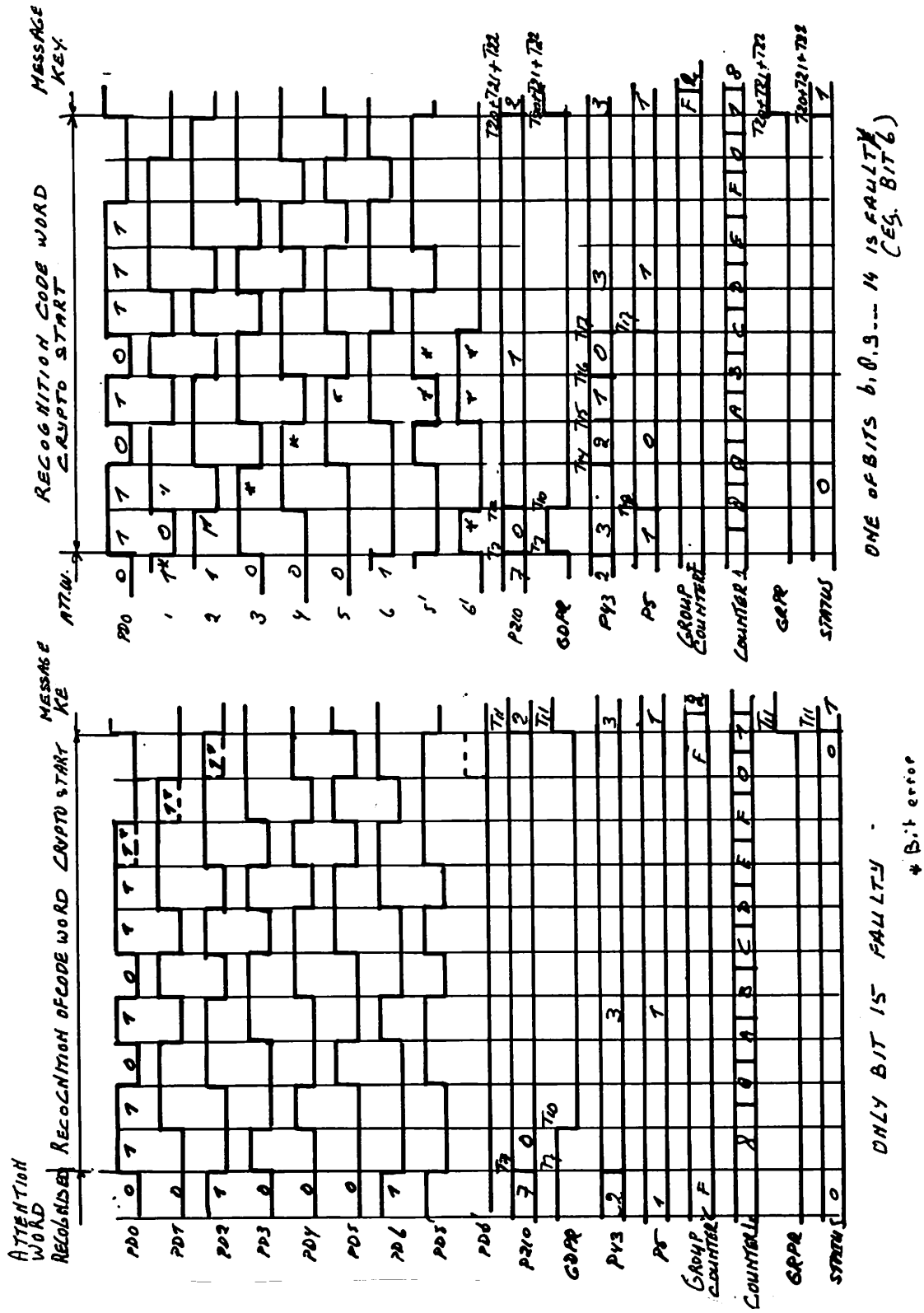


Figure 2.4-3 a and b: Pulse diagram, recognition of code word crypto start

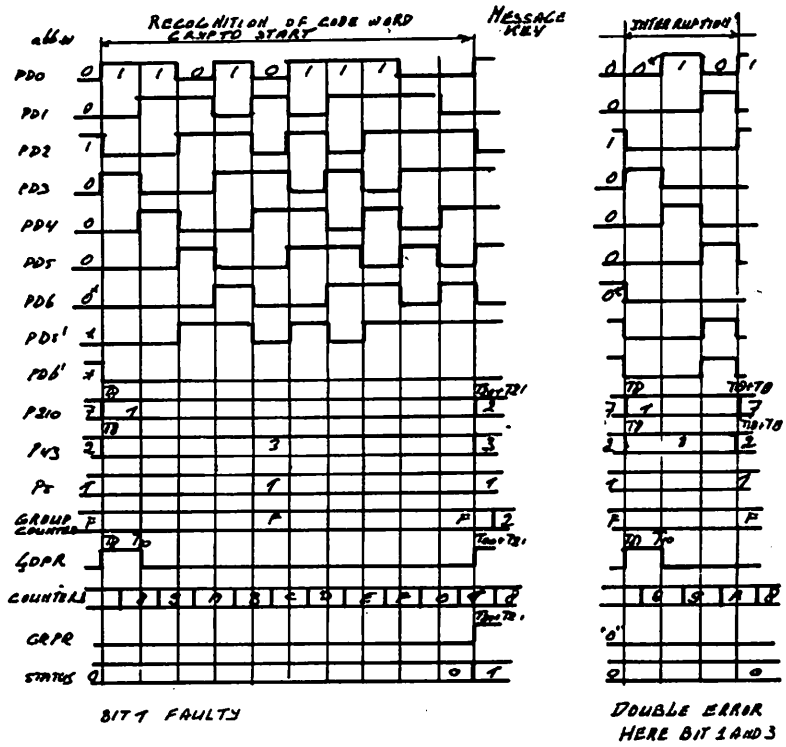


Figure 2.4-3c: Pulse diagram, recognition of code word crypto start (continued)

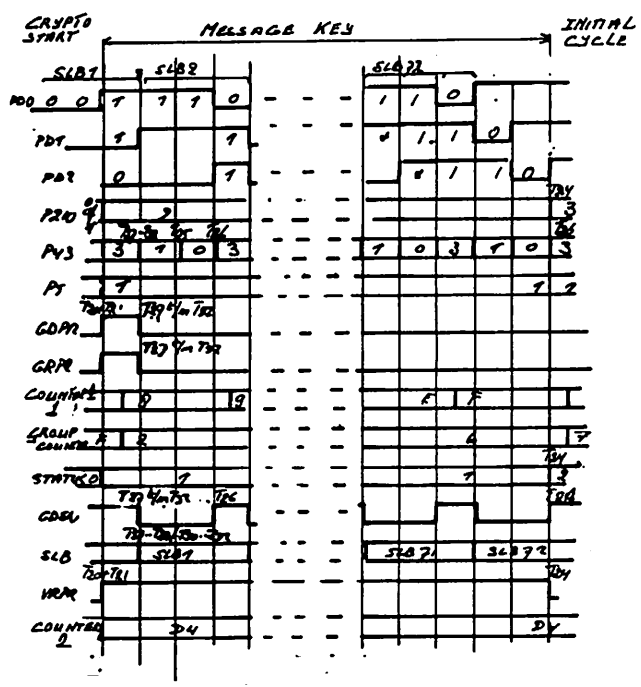


Figure 2.4-4: Pulse diagram, decoding of message key

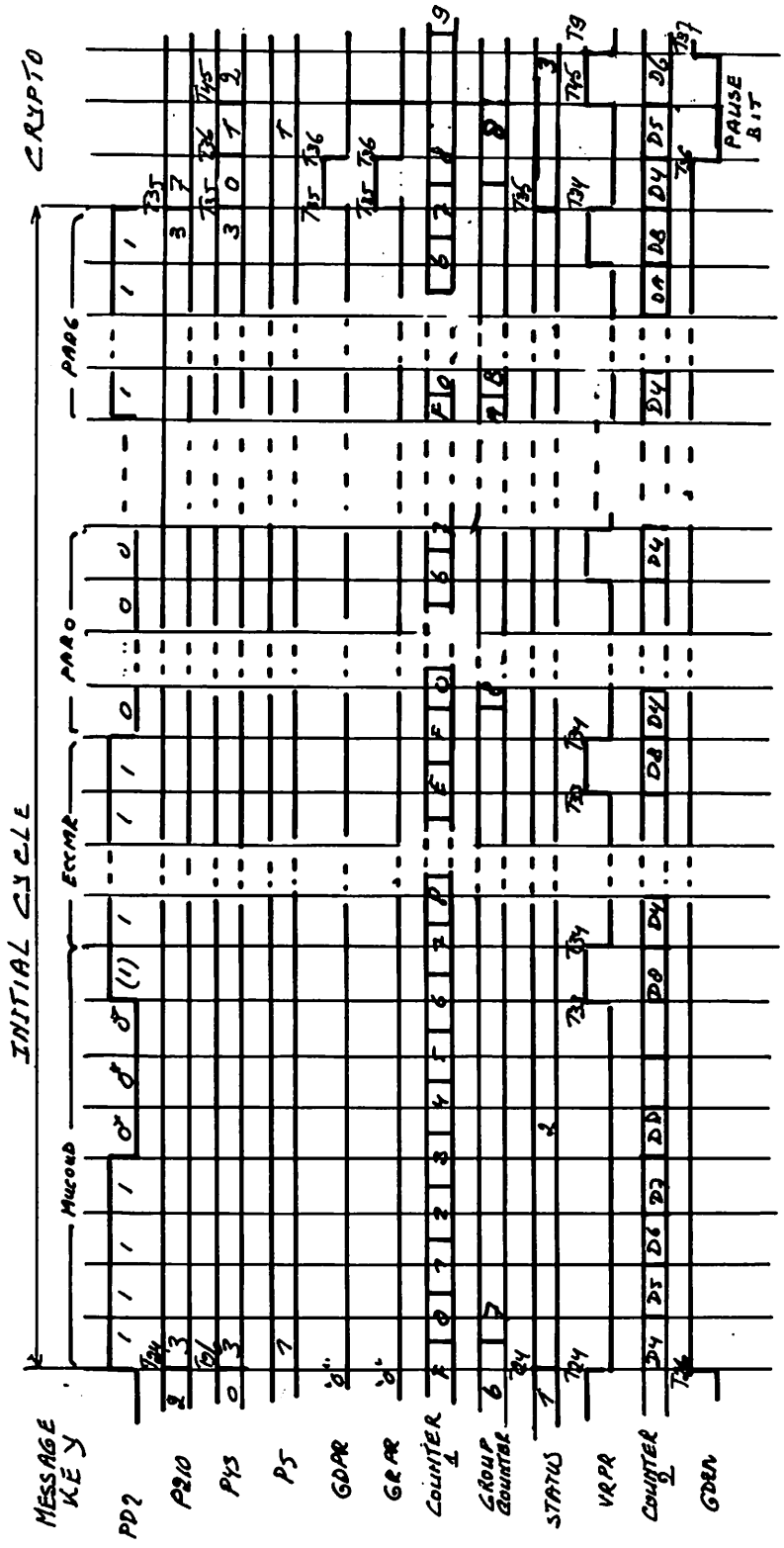


Figure 2.4-5: Pulse diagram, initial cycle

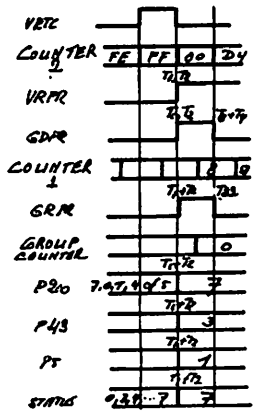


Figure 2.4-6: Pulse diagram, counter 2 in final position

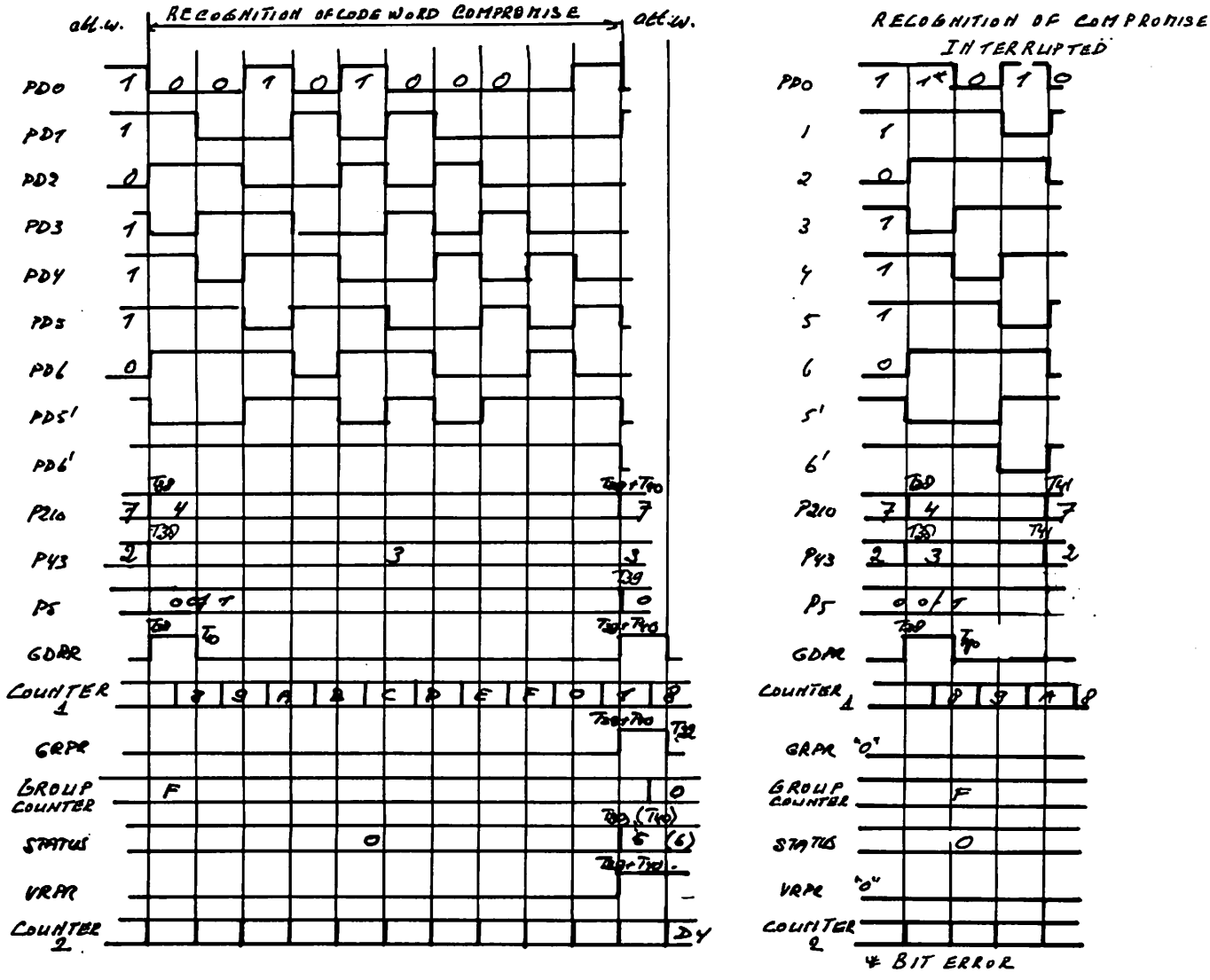


Figure 2.4-7: Pulse diagram, recognition of code word compromise

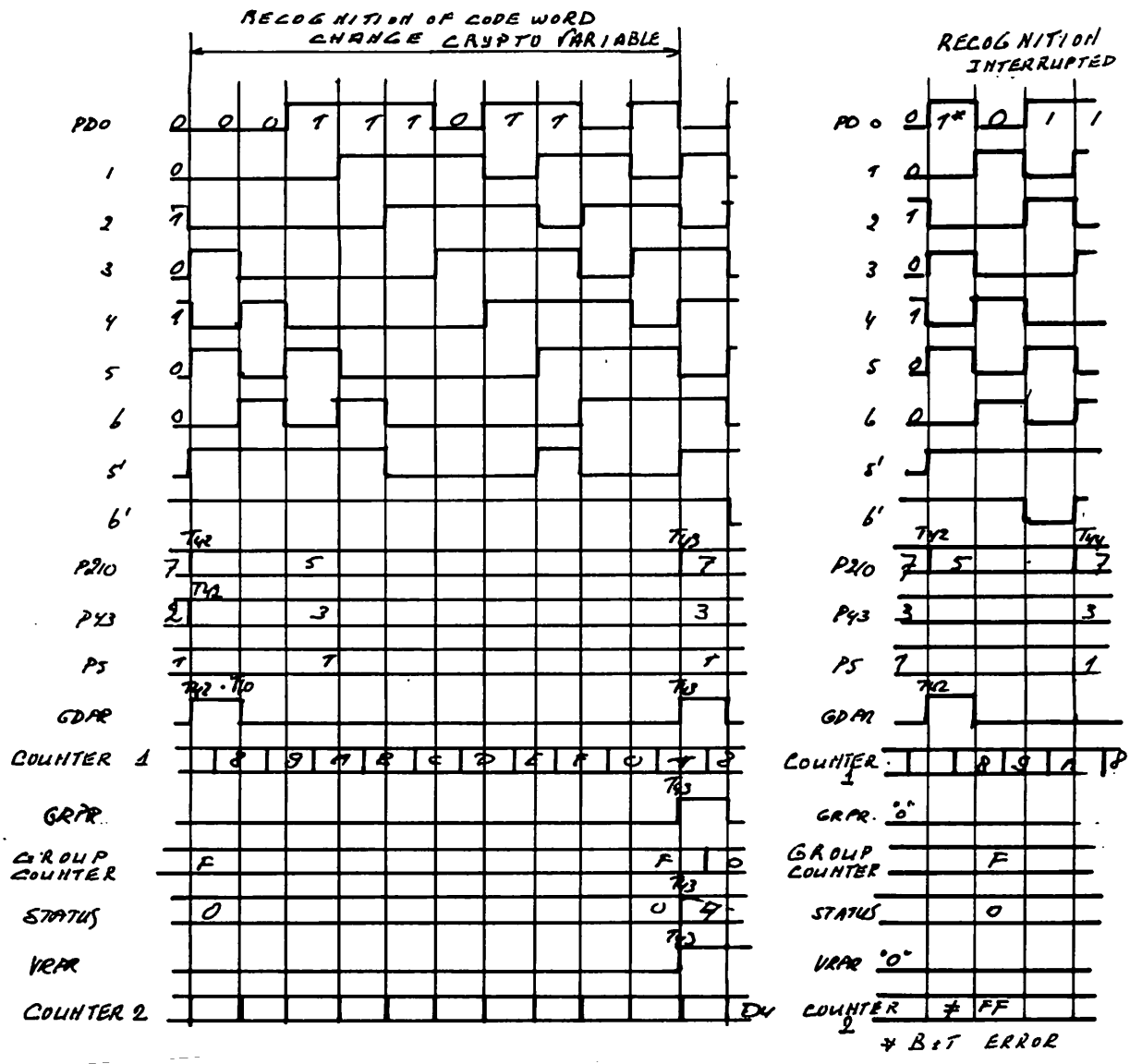


Figure 2.4-8: Pulse diagram, recognition of crypto variable

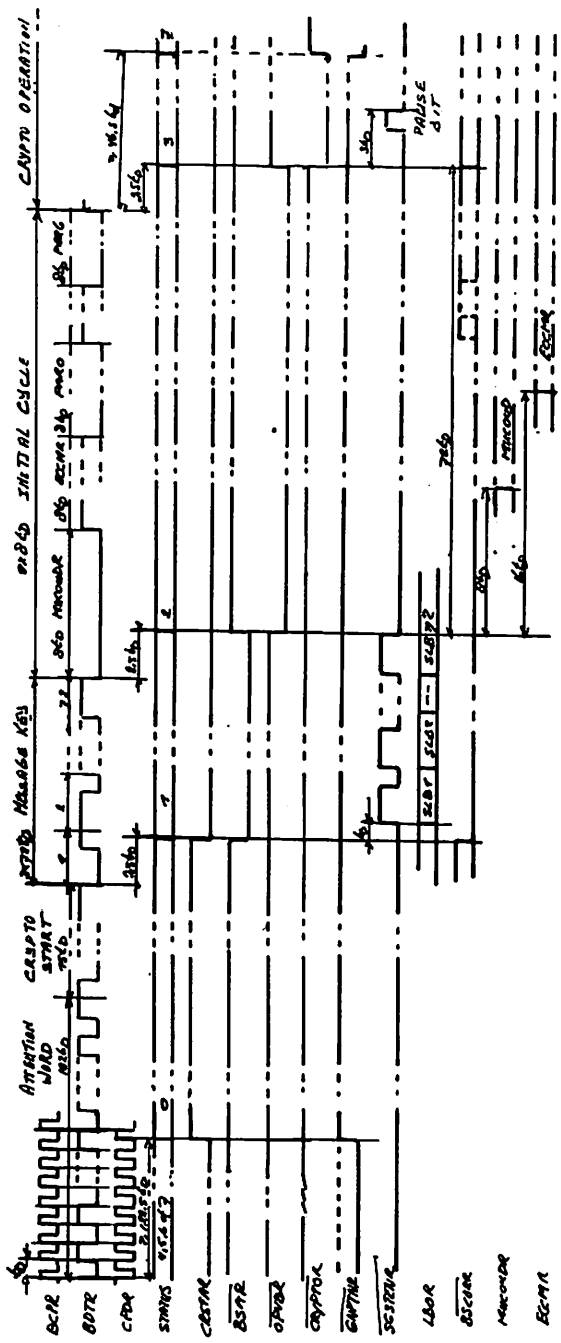


Figure 2.4-9: Pulse diagram, interface signals during crypto start

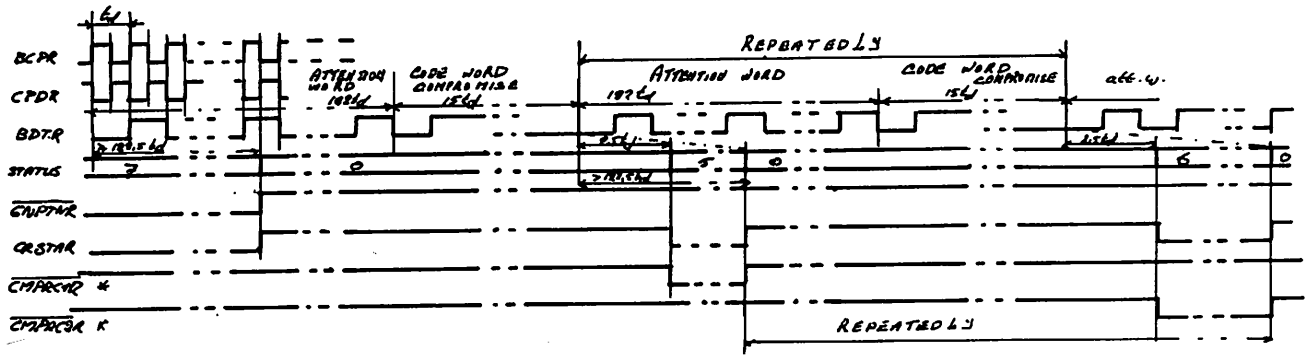


Figure 2.4-10: Pulse diagram, interface signals during recognition of compromise

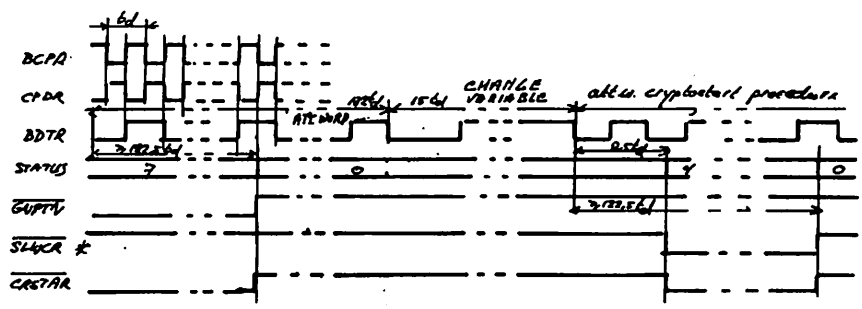


Figure 2.4-11: Pulse diagram, interface signals during recognition of change crypto variables

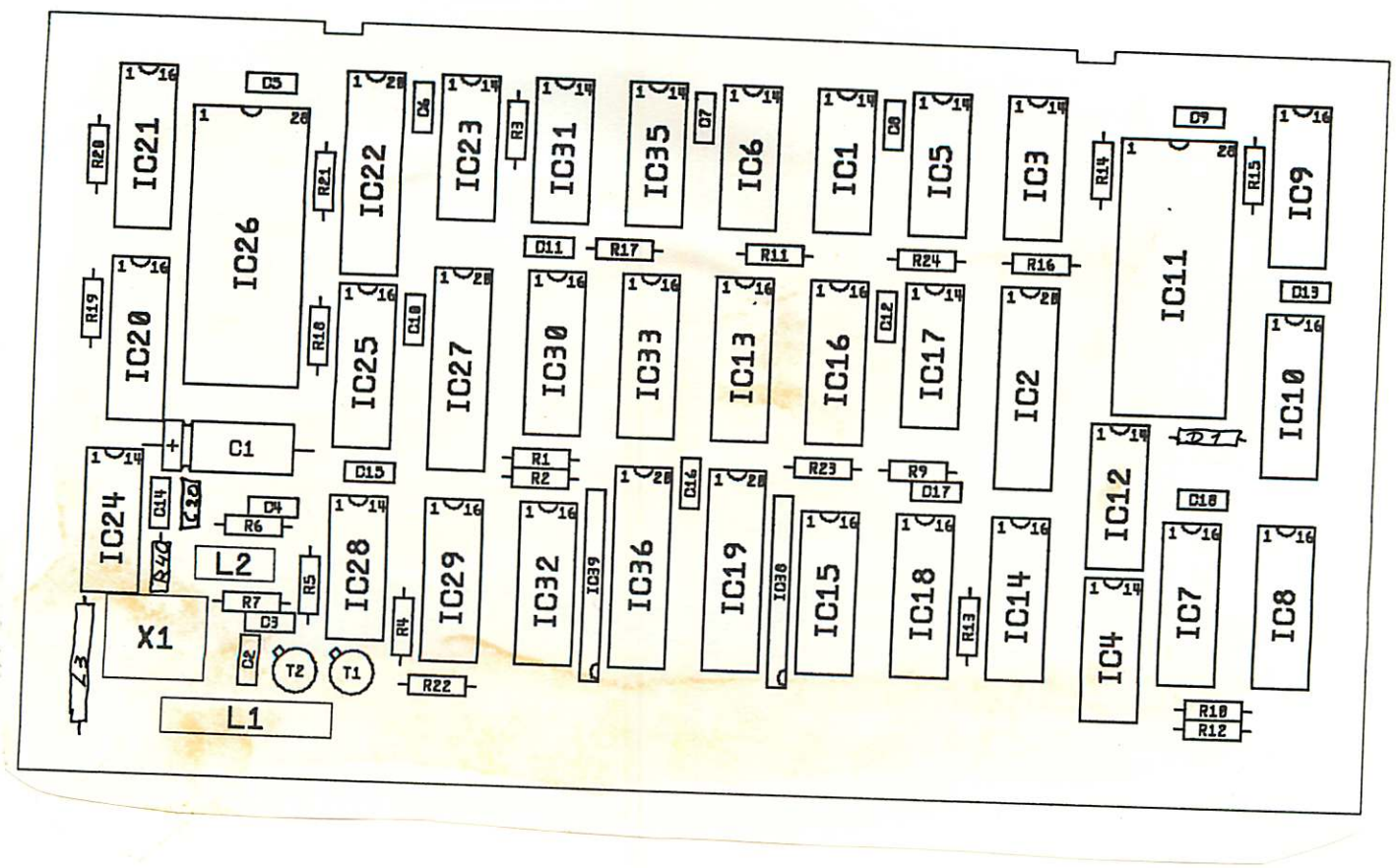


Figure 2.4-13: Pattern unit panel

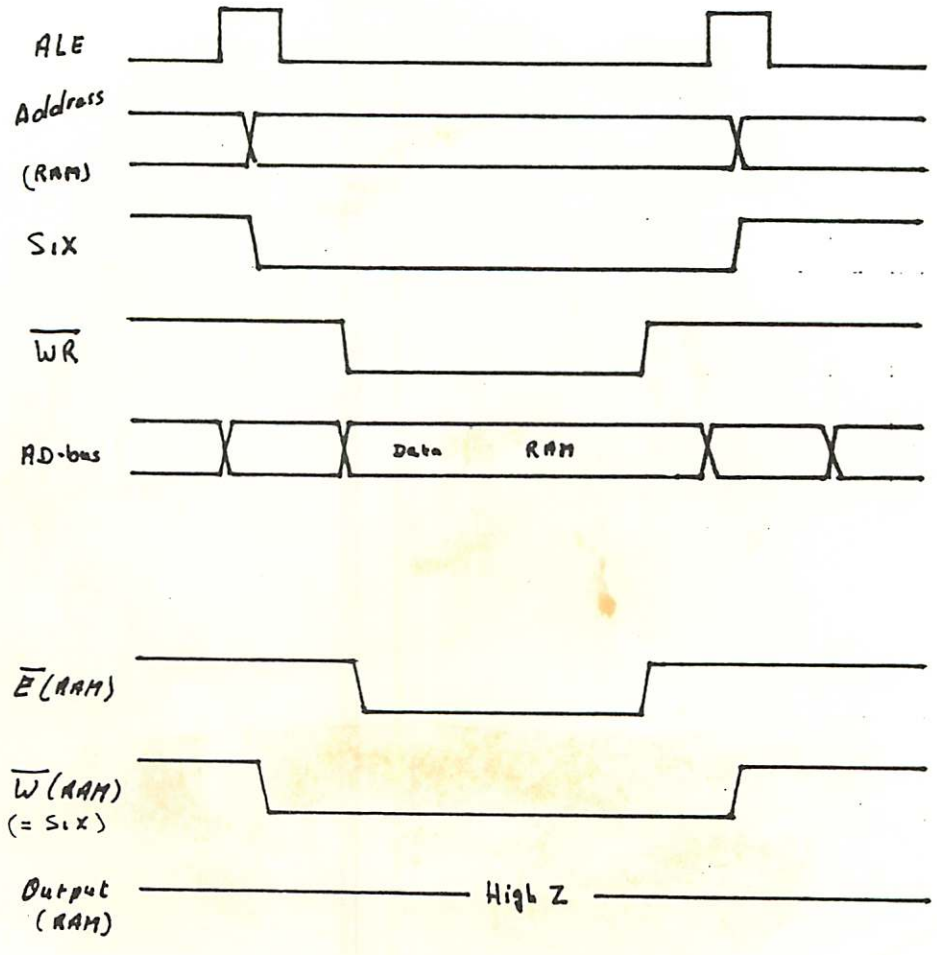


Figure 2.6-1: Pulse diagram, write cycle of CMOS RAM

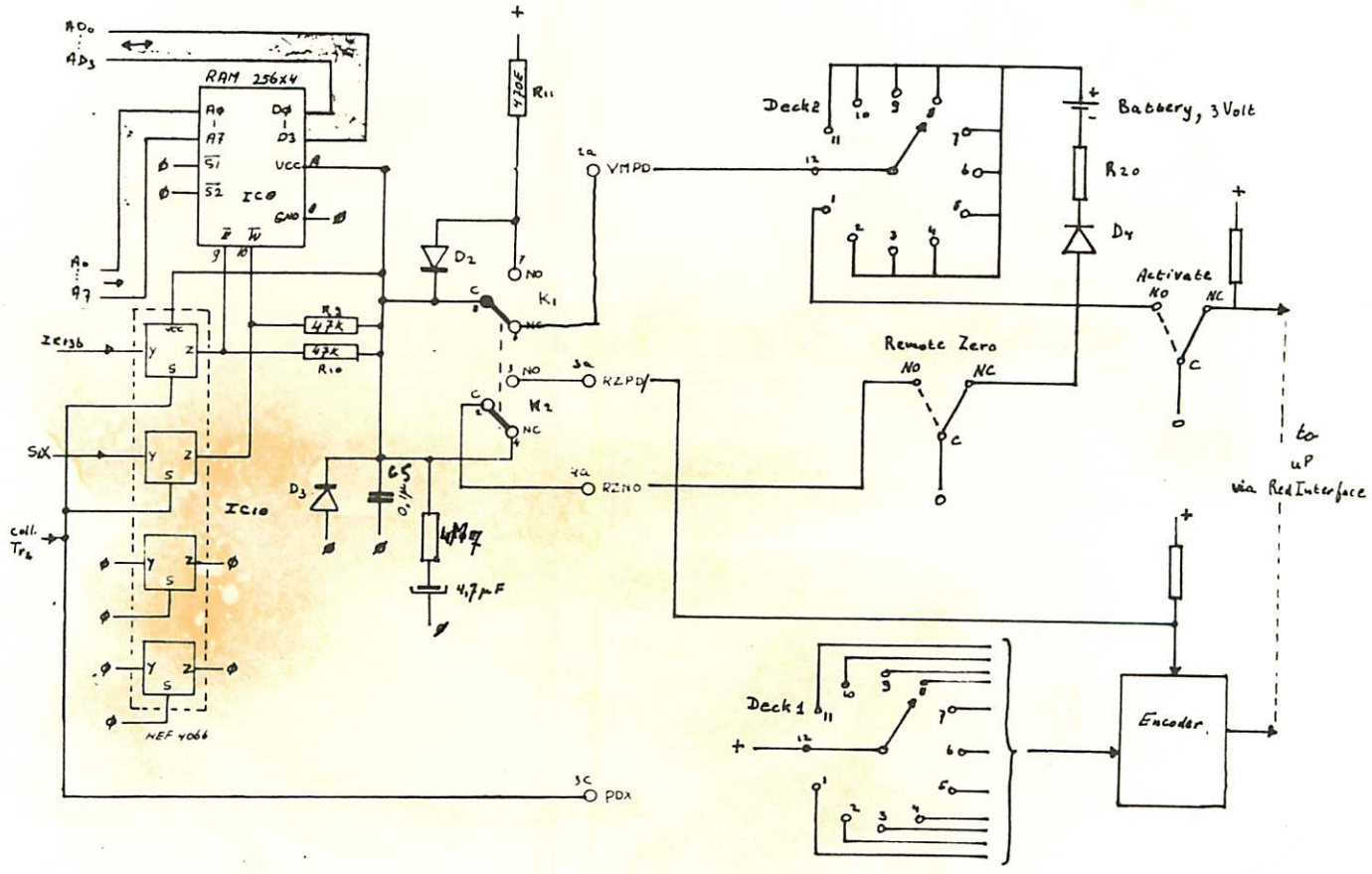
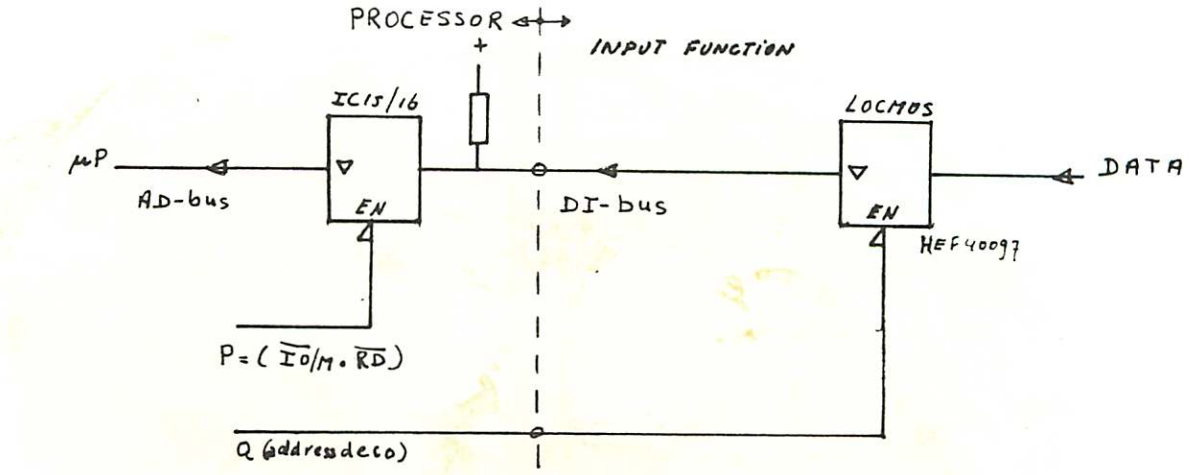
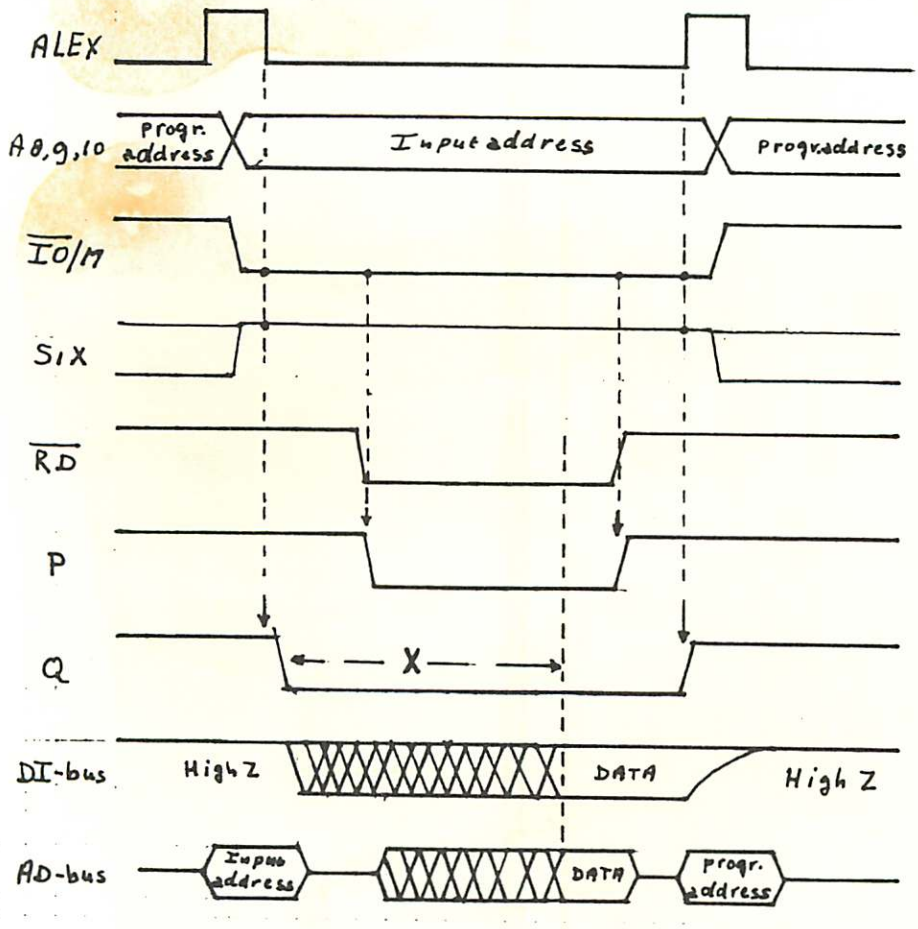


Figure 2.6-2: Key memory control





Note: X is the max. possible enable time for the LOCMOS buffers. In worst case this time is 735 ns. As only 200ns are needed to enable the buffers, 535 ns remain in reserve.

Figure 2.6-3: Timing diagram addressing of input buffers

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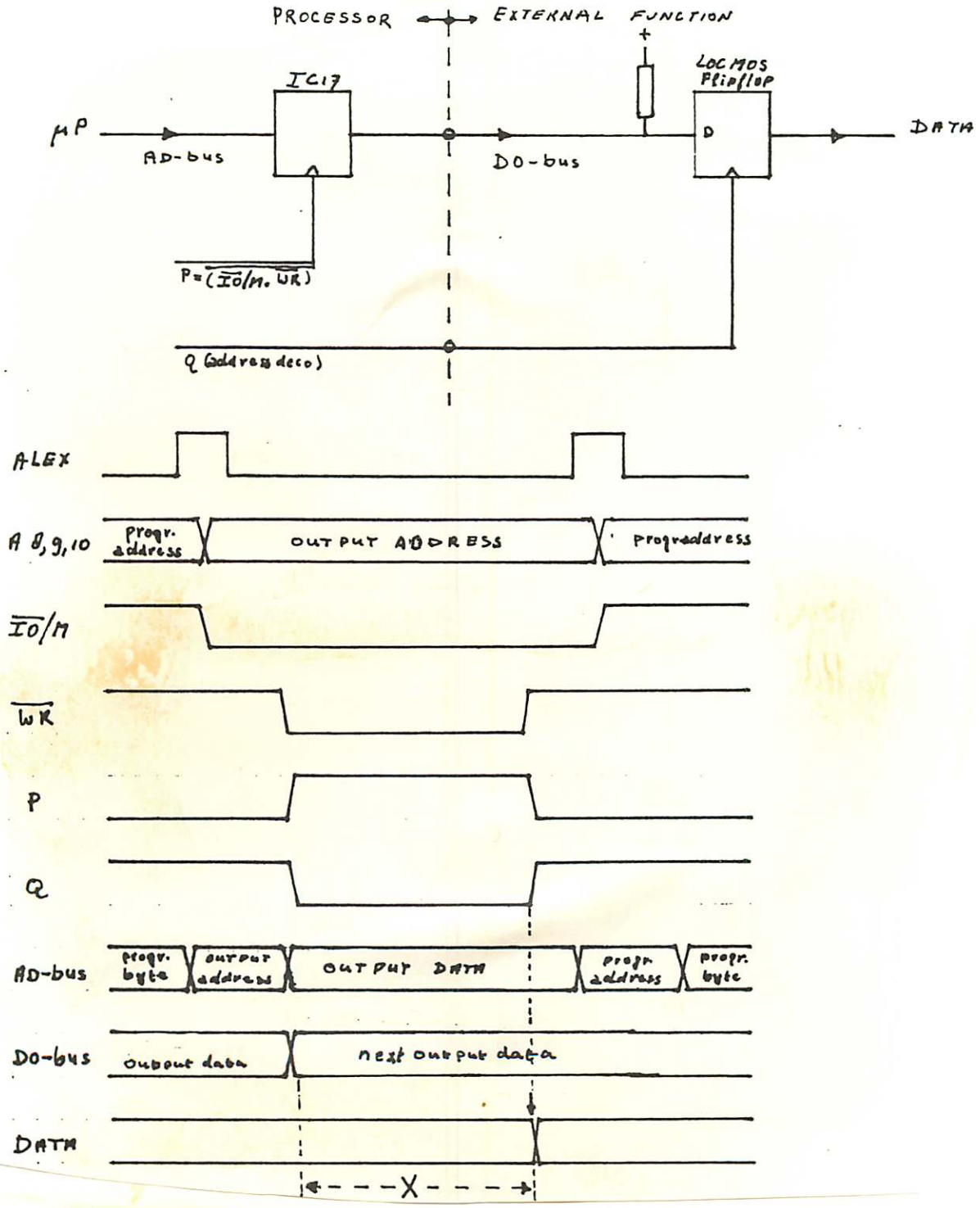
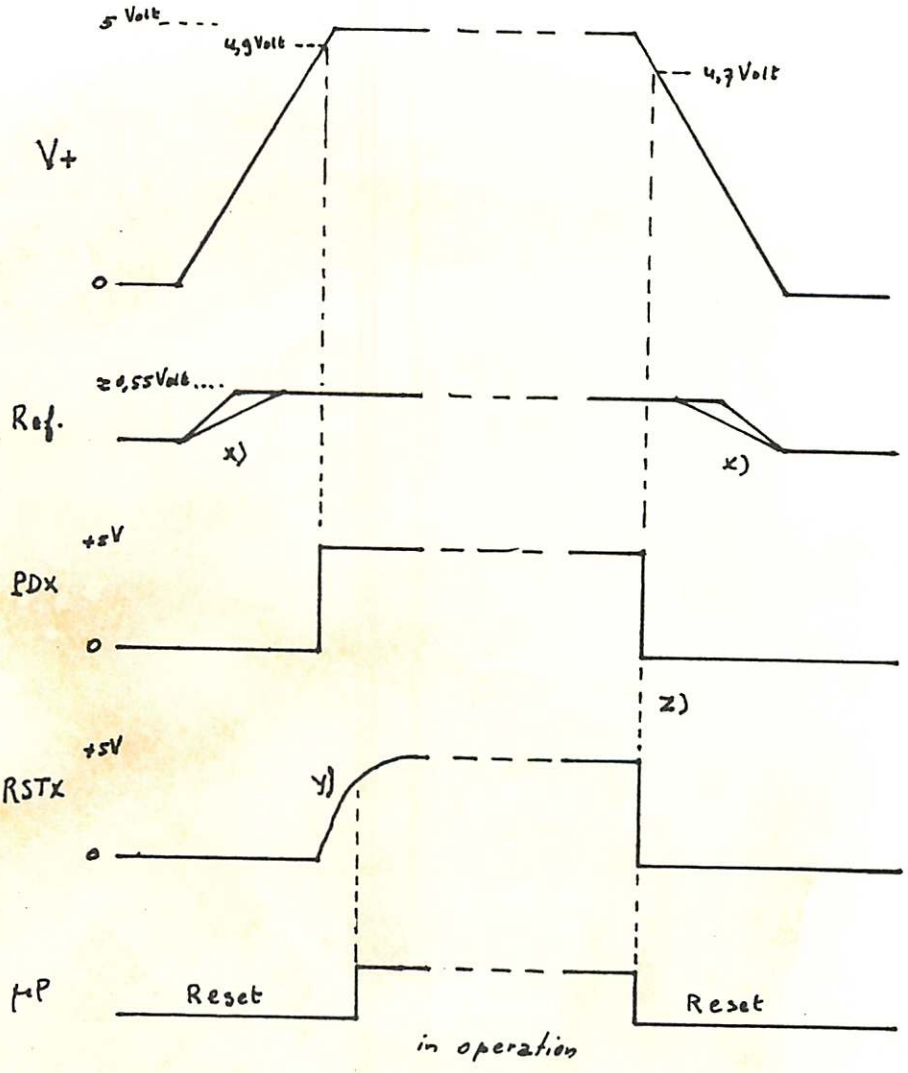


Note: X is the set-up time for the LOCMOS flip-flops.
In worst case the minimum set-up time is 621 ns.
As only 60 ns are needed to set up the flip-flops
561 ns remain in reserve.

Figure 2.6-4: Timing diagram addressing of output flip-flops



X) Tolerance Tr 1

Y) RC-time 10 msec nominal

z) Delay PDX ↓ ... RSTX ↓ : ± 5 μsec max.

Figure 2.6-5: Circuit diagram, reset/power down circuit

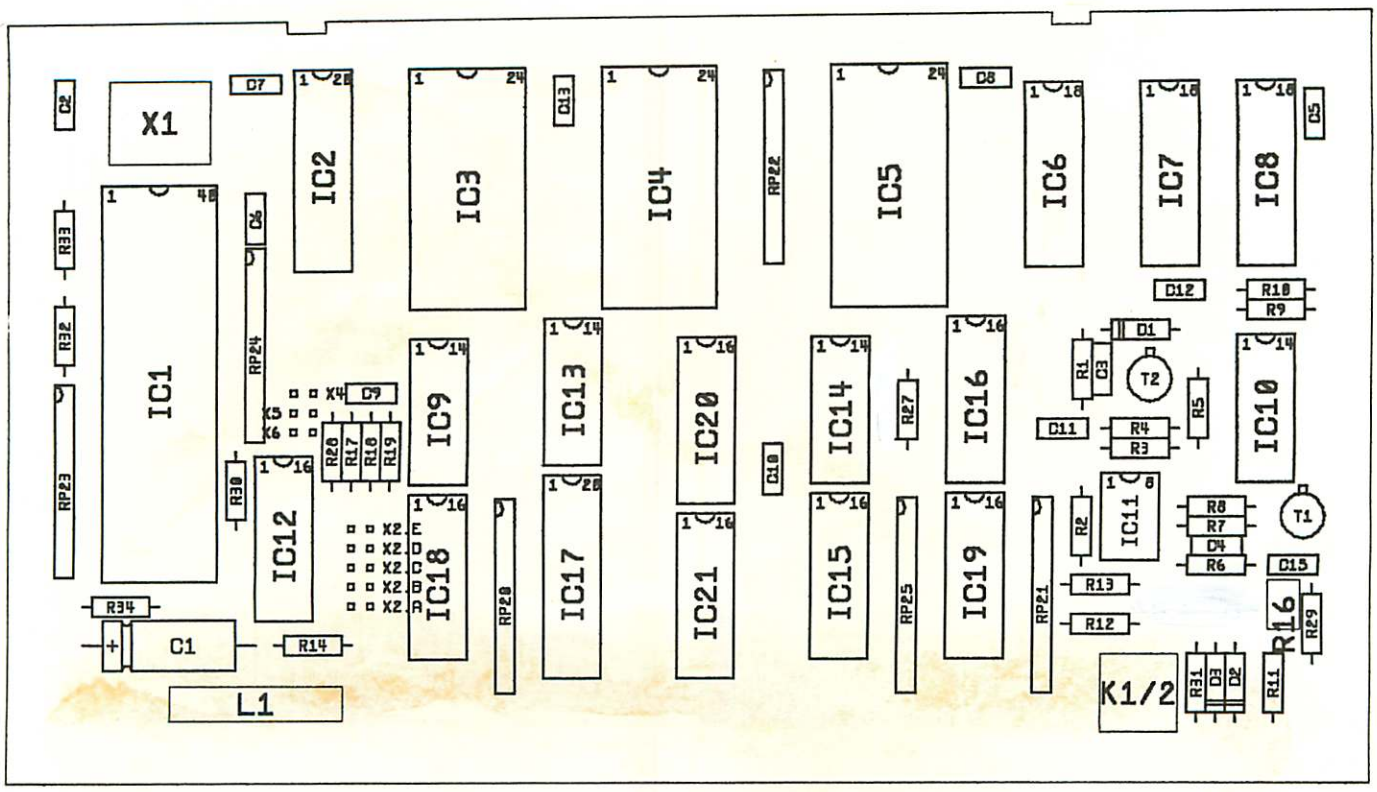


Figure 2.6-7: Processor panel

		PRESENT P						INPUTS								NEXT P						OUTPUT				
T	C IN	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0	C OUT
0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	i	0	0	i	i	i	i	0	i	i	i	i	.
1	.	.	.	.	.	.	.	0	0	0	.	.	.	.	.	.	.	.	.	.	.	.	.	1	0	1	1	1	1	1	0	0	1	1	1	1	.
2	.	.	.	.	.	.	.	0	0	1	.	.	.	.	.	.	.	.	.	.	.	.	.	1	0	1	1	1	1	1	0	0	1	1	1	1	.
3	.	.	.	.	.	.	.	0	1	0	.	.	.	.	.	.	.	.	.	.	.	.	.	1	0	0	0	1	1	1	0	0	1	1	1	1	.
4	.	.	.	.	.	.	.	0	1	1	.	.	.	.	.	.	.	.	.	.	.	.	.	1	1	0	1	1	1	1	0	1	0	1	1	1	.
5	.	i	i	i	i	i	i	1	.	.	i	.	.	.	.	ò	ò	i	i	ò	ò	ò	ò	1	i	1	0	0	0	1	0	1	0	.	1	1	.
6	.	0	.	.	0	0	0	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	.	.	0	0	0	1	1	1	0	0	1	1	.
7	.	1	.	.	0	0	0	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0	.	.	ò	0	ò	1	1	1	.	1	0	0	.
8	.	1	.	.	0	0	0	1	.	.	.	.	.	.	.	1	1	1	0	1	0	1	1	0	.	.	0	0	0	1	1	1	1	0	1	0	0	.
9	.	0	.	.	0	0	0	1	.	.	.	.	.	.	.	1	1	1	0	1	1	0	0	1	i	i	0	0	0	1	1	1	0	1	1	0	0	.
10	.	0	i	i	0	0	0	1	.	.	.	.	.	.	.	1	1	1	0	1	1	1	0	1	i	i	0	0	0	1	1	1	0	1	1	0	0	.
11	.	1	1	1	0	0	1	1	.	.	.	.	0	.	.	.	.	.	.	.	.	.	.	1	1	1	0	0	0	1	1	1	0	1	1	0	0	.
12	.	1	1	1	0	0	1	1	.	.	.	.	.	1	.	.	.	.	.	.	.	.	.	1	.	.	0	.	.	1	1	0	1	1	0	0	1	.
13	.	1	1	1	0	0	1	1	.	.	.	.	.	1	.	i	i	i	i	i	i	ò	i	1	ò	ò	0	i	ò	1	1	0	1	1	0	0	1	.
14	.	.	0	0	0	1	0	1	.	.	.	.	.	.	0	.	.	.	.	.	.	.	.	0	0	1	0	1	0	0	0	1	1	0	1	0	1	0	.
15	.	.	0	0	0	1	0	1	.	.	.	.	.	.	1	.	.	.	.	.	.	.	.	1	0	1	0	1	0	0	0	1	1	1	1	0	1	0	.
16	.	.	0	1	0	1	0	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	1	0	1	0	1	1	1	0	0	0	1	0	.
17	.	ò	1	1	0	1	0	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0	0	0	1	1	.	.	.	1	0	0	1	0	.
18	.	1	1	1	0	1	0	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0	0	0	0	1	1	ò	ò	1	0	0	0	1	0	.
19	.	.	1	1	0	1	0	1	.	.	.	.	.	.	.	ò	ì	ò	ò	ò	ì	ì	ì	ò	ò	1	.	0	0	0	1	0	0	0	1	0	.
20	.	.	0	0	0	1	1	1	.	.	.	.	.	.	.	0	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	.
21	.	i	1	1	0	1	1	1	.	.	.	.	.	.	ò	0	0	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	.
22	.	1	1	1	0	1	1	1	.	.	.	.	.	.	1	0	0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	.
23	.	1	1	1	0	1	1	1	.	.	.	.	.	.	.	0	1	.	.	.	1	1	0	1	1	1	.	1	1	1	1	1	1	.	1	0	1	1	.
24	.	1	1	1	0	1	1	1	.	.	.	.	.	0	.	0	1	.	.	.	1	1	0	1	1	1	0	1	1	1	0	1	1	0	1	0	1	1	.
25	.	1	1	1	0	1	1	1	.	.	.	.	.	1	.	0	1	.	.	ò	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	.
26	.	1	1	1	0	1	1	1	.	.	.	.	.	.	.	0	1	i	i	0	1	1	0	1	1	1	.	1	1	1	1	1	1	1	1	0	1	1	.
27	.	1	1	1	1	1	1	1	.	.	.	.	.	.	.	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	.
28	.	1	1	1	1	1	1	1	.	.	.	.	.	.	.	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	.
29	.	1	0	0	1	1	1	1	.	.	.	.	.	.	.	0	1	1	1	1	0	0	1	1	1	0	1	1	1	0	0	1	1	1	1	1	1	.
30	.	1	0	.	1	1	1	1	.	.	.	.	.	.	.	0	0	1	1	0	0	0	0	1	1	0	.	1	0	0	1	1	1	1	1	1	1	.
31	.	0	0	i	0	0	0	1	.	.	.	.	.	.	.	1	1	1	0	1	1	1	1	1	0	i	1	0	0	1	1	1	0	0	1	1	1	.
32	.	1	0	1	1	0	1	1	.	.	.	.	.	0	.	.	.	.	.	.	.	.	.	1	0	1	1	0	1	1	1	1	1	1	1	0	1	.
33	.	1	0	1	1	0	1	1	.	.	.	.	.	1	.	.	.	.	.	.	.	.	.	1	0	1	.	0	.	1	.	0	0	1	1	0	1	.
34	.	1	0	1	1	0	1	1	.	.	.	.	.	1	.	i	i	i	i	i	i	0	i	1	0	1	0	0	0	1	1	0	0	1	1	0	1	.
35	.	1	0	0	0	0	0	1	.	.	.	.	.	.	.	1	1	1	0	1	1	0	0	0	0	1	0	0	0	1	1	0	0	1	1	0	0	.
36	.	0	0	0	0	0	0	1	.	.	.	.	.	.	.	1	1	1	0	1	1	1	0	1	0	0	1	0	0	1	1	1	1	1	0	0	0	.
37	.	1	0	0	1	0	0	1	.	.	.	.	.	0	.	.	.	.	.	.	.	.	.	1	0	0	0	.	0	0	0	1	1	1	1	0	0	.
38	.	1	0	0	1	0	0	1	.	.	.	.	.	1	.	i	i	i	i	i	i	0	i	1	0	0	0	0	0	1	1	0	0	1	1	0	0	.
39	.	1	0	0	1	0	0	1	.	.	.	.	.	0	.	i	i	i	i	i	i	ò	i	1	0	0	1	0	0	0	1	0	1	1	0	0	0	.
40	.	1	0	0	0	0	0	1	.	.	.	.	.	.	.	1	1	1	1	1	1	1	0	0	1	1	0	0	0	1	1	1	1	1	0	0	0	.
41	.	1	1	1	0	0	1	1	.	.	.	.	.	ò	.	0	0	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1	0	1	1	.
42	.	1	1	1	0	1	1	1	.	.	.	.	.	1	.	0	0	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	1	1	.
43	.	1	1	1	1	1	1	1	.	.	.	.	.	.	.	0	1	1	1	1	1	0	1	1	0	0	1	1	0	1	1	0	1	0	1	1	1	.
44	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
45	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
46	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
47	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.

Table 2.3-1: AND and OR programming of FPLS (pattern generator)

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

		PRESENT P						INPUTS									NEXT P						OUTPUT				
T	C IN	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0	C OUT
0	.	.	.	.	0	0	.	0	1	1	1	1	0	0	0	1	.	.	.	.	.	.	.																
1	.	.	.	.	.	0	1	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	.
2	.	.	i	.	i	1	i	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	.
3	.	.	1	.	1	1	1	0	.	.	.	.	.	i	0	0	0	i	i	0	i	0	i	.	1	.	1	1	1	.	0	0	1	1	.	.	.	.
4	.	.	1	.	1	1	1	0	.	.	.	.	.	1	0	0	0	1	1	0	1	0	1	0															
5	.	.	1	.	1	1	1	0	.	.	.	.	.	.	.	.	.	.	0	.	.	.	.	.	1	.	.	.	1	.	0	0	1	1	1	.	.	.	.
6	.	.	1	0	1	1	1	0	.	.	.	.	.	1	1	1	i	.	.	.	.	.	.	.	1	.	.	.	1	.	i	0	1	1	1	.	.	.	.
7	.	i	1	0	1	1	1	0	i	i	i	i	i	.	.	.	.	0	i	0	i	.	0	1	i	1	i	0	0	0	.	0	1	1	1	0	0	0	.
8	.	1	1	0	1	1	1	0	1	1	1	1	1	.	.	.	.	1	0	0	0	1	0	0	1	1	1	0	0	1	1	0	1	1	1	0	0	0	.
9	.	.	1	0	1	1	1	0	0	.	.	.	.	i	0	0	0	.	.	.	.	.	.	.	.	1	.	.	.	.	0	0	1	1	.	.	.	.	.
10	.	.	1	1	.	0	.	0	i	i	i	i	i	1	0	0	0	.	.	.	.	.	.	.	.	1	.	.	.	.	0	0	0	1	1	0	0	0	.
11	.	i	1	1	0	0	0	0	1	1	1	1	1	0	0	0	1	.	.	.	.	.	.	.	i	1	1	1	0	i	0	1	1	1	0	0	1	.
12	1	1	1	1	0	0	0	0	1	1	1	1	1	.	.	.	1	.	.	.	.	.	.	0	1	1	0	0	1	1	0	0	0	1	1	0	0	0	.
13	1	1	1	0	1	1	1	0	0	1	1	1	1	i	0	0	0	.	.	.	.	.	.	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	.
14	1	0	1	1	0	0	1	0	1	1	1	1	1	.	.	.	0	.	.	.	.	.	.	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	.
15	1	0	1	0	0	0	1	0	1	1	1	1	1	.	.	.	0	.	.	.	.	.	.	0	0	1	0	0	1	1	0	0	0	0	1	0	0	0	.
16	1	0	0	1	0	0	1	0	1	1	1	1	1	.	.	.	1	.	.	.	.	.	.	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	.
17	1	0	0	0	0	0	1	0	1	1	1	1	1	.	.	.	1	.	.	.	.	.	.	1	1	1	0	0	1	1	0	0	0	0	1	1	0	0	.
18	.	.	1	.	0	0	1	0	1	1	1	1	1	.	.	.	1	.	.	.	.	.	.	1	1	0	1	1	1	0	0	0	1	1	0	0	0	.
19	.	.	0	.	0	0	1	0	1	1	1	1	1	.	.	.	0	.	.	.	.	.	.	1	1	0	1	1	1	0	0	1	1	0	0	0	0	.
20	.	.	1	.	0	0	1	0	1	1	1	1	1	0	0	0	1	0	.	.	.	.	.	1	1	1	0	1	0	1	1	1	1	1	0	0	1	.
21	.	.	0	.	0	0	1	0	1	1	1	1	1	0	0	0	1	1	.	.	.	.	.	1	1	1	0	1	0	0	1	1	1	1	0	0	1	.
22	.	.	1	1	1	1	1	0	.	.	.	.	.	1	0	0	0	.	.	.	.	.	.	.	1	1	1	1	1	1	1	0	1	1	1	.	.	.	.
23	.	.	1	1	1	1	1	0	.	.	.	.	.	1	1	1	1	.	.	.	.	.	.	.	1	0	1	1	1	1	i	0	1	1	1	.	.	.	.
24	.	1	0	0	0	1	0	.	0	1	1	1	0	1	1	1	1	.	.	.	.	.	.	1	1	1	0	0	1	1	0	0	0	1	0	.	0	1	0	.
25	.	1	0	1	0	1	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	0	0	0	1	1	0	1	0	0	0	1	0	.	0	0	1	.
26	.	1	0	0	0	1	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	1	1	0	0	1	.	0	0	0	1	.	0	0	.	.
27	.	1	1	1	0	1	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0	1	0	1	0	.	0	0	0	0	0	0	0	i	.
28	.	1	1	1	0	1	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0	1	1	0	1	0	1	0	1	0	0	0	0	0	0	1	.
29	.	1	1	1	0	1	0	.	.	.	.	.	.	.	.	.	.	.	.	.	0	.	1	1	0	1	0	1	0	1	0	0	0	0	0	0	1	.
30	.	1	1	1	0	1	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	1	.
31	.	1	1	1	0	1	0	.	.	.	.	.	.	.	.	.	.	.	.	.	i	.	0	1	0	1	0	1	0	1	0	0	0	0	0	0	1	.
32	.	1	1	1	0	1	0	.	.	.	.	.	.	.	.	.	.	.	.	.	1	1	.	1	0	1	0	1	0	1	0	0	0	0	1	0	0	1	.
33	.	1	1	1	0	1	1	.	.	.	.	.	.	.	i	i	0	.	.	.	.	.	.	1	1	1	0	1	1	1	0	0	0	1	1	0	1	0	.
34	.	1	1	1	0	1	1	.	.	.	.	.	.	.	1	1	1	.	.	.	.	.	.	1	.	.	.	.	1	1	0	0	0	0	1	0	1	1	.
35	.	1	1	1	0	1	1	.	i	0	i	i	0	1	1	1	.	.	.	.	.	.	.	1	0	0	i	1	1	0	0	i	i	1	1	0	1	i	.
36	.	1	0	0	1	1	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	0	1	1	1	1	0	0	0	0	1	0	1	1	.
37	.	1	1	0	1	1	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	1	.	.	.	.	.	0	.	0	1	1	0	0	0	.
38	.	.	1	0	1	1	1	0	i	i	i	i	i	.	.	.	.	.	i	i	i	.	.	.	.	1	1	1	1	i	0	i	1	1	0	0	0	.
39	.	i	1	1	1	0	0	0	1	1	1	1	1	1	0	0	0	i	1	.	.	.	.	.	0	1	1	1	1	1	i	1	1	1	1	0	0	1	.
40	.	0	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	.	.	.	.	.	0	1	1	1	1	1	1	1	1	1	1	1	1	0	.
41	.	.	1	1	1	0	0	0	1	1	1	1	1	.	.	.	1	0	.	.	.	.	.	1	1	0	1	1	1	0	0	0	1	1	0	0	0	.
42	.	i	1	0	1	1	1	0	1	1	1	1	1	.	.	.	1	1	0	i	.	.	.	0	1	1	1	1	0	1	1	1	1	1	0	0	0	.
43	.	1	1	1	1	0	1	0	1	1	1	1	1	0	0	0	1	1	.	.	.	.	.	1	1	1	1	1	1	1	1	1	1	1	1	0	0	.
44	.	1	1	1	1	0	1	0	1	1	1	1	1	.	0	.	.	.	.	.	.	.	.	1	1	0	1	1	1	0	0	0	1	1	0	0	0	.
45	.	1	0	1	1	1	1	0	.	.	.	.	.	.	0	0	0	.	.	.	.	.	.	1	1	0	1	1	1	1	0	0	0	1	1	0	1	.
46	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
47	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.

Table 2.4-1: And and OR programming of FPLS (pattern recognition)

DESCRIPTION INTERCONNECTION PANEL BVO-M: 4322 082 56490

The panel is described by:
1 List of connector pins, the interconnections and the belonging signal names.
2 Scheme of connections between the pattern unit and the 6 PCBs of the key generators.

ad 1 and 2:
The etched wiring of the panel connects in principle signals with identical names. However this is not done consequently because PCB key generator I is used 4 times and PCB key generator II is used 2 times.
PCB key generator I: Wheels numbered 1 through 4 and wheels 5 through 8 as transmitter or as receiver key generator.
PCB key generator II: Wheel 9, control and ECCM circuit as transmitter or as receiver key generator.
The signal names on the PCBs are mostly mnemonics of the functions (mostly in Dutch). For this reason, the interconnections are not only listed but also drawned, see figure 3.1.

Indications:
Voeding means: power supply.
n.c.: not connected output signal.
n.c.(+): not connected input signal (the input is made "high")

Key-posities X10 t/m X19:

Connector	Key			
X10	6		X15	1,10
X11	1,7		X16	1,8
X12	1,8		X17	1,8
X13	1,8		X18	1,9
X14	1,9		X19	11

Table 3: List of connectors, pin no. signal names and interconnections on interconnection panel.

NATO CONFIDENTIAL

NARRATIVE DESCRIPTION OF MUCOLEX - II

Connector X3
(Black filter compartment)

pin	signal	connected to
X3-01	VB	X19-32a, -32c
X3-02	VB	X19-32a, -32c
X3-03	LASE	X19-19c
X3-04	LASC	X19-20c
X3-05	ALC	X19-08c
X3-06	ALNO	X19-06c
X3-07	ALNC	X19-07c
X3-08	GND	ground
X3-09	GND	ground
X3-10	BL1	X19-12a
X3-11	BL2	X19-13c
X3-12	BSG2	X19-14c
X3-13	BSG1	X19-04c
X3-14	BSC	X19-15c
X3-15	BL3	X19-02c
X3-16	BL4	X19-03c

Connector X5
(Red filter compartment)

pin	signal	connected to
X5-01	LASO	X19-20a
X5-02	GND	ground
X5-03	STNM/	X10-26b
X5-04	RZNO	X11-04a
X5-05	STSN/	X10-24b
X5-06	STBV/	X10-25b
X5-07	RL2	X10-29a
X5-08	RL1	X10-30a
X5-09	RSG1	X10-26a
X5-10	RL5	X10-28a
X5-11	RSG2	X10-24a
X5-12	SYNC2/	X10-25a
X5-13	RL4	X10-22a
X5-14	RL3	X10-23a
X5-15	GND	ground
X5-16	RZNC	X8-01

Connector X9 (voeding)	V+	X10-32a,-b,-c, X11-32a,-c, X12-32a,-c, X13-32a,-c, X14-32a,-c, X15-32a,-c, X16-32a,-c, X17-32a,-c, X18-32a,-c

Table 3-1: Connector X3, connector X5 and X9

Connector X8
(Front)

pin	signal	connected to
X8-01	RZNC	X5-16
X8-02	FDCV	X10-07a
X8-03	FDSL	X10-06a
X8-04	FDRY/	X10-04a
X8-05	FDCP	X10-03a
X8-06	FDDT	X10-02a
X8-07	GND	ground
X8-08	GND	ground
X8-09	FTPS	X10-19a,-20a
X8-10	FTPS	X10-19a,-20a
X8-11	DPA5	X10-09a
X8-12	DPA4	X10-10a
X8-13	DPA3	X10-12a
X8-14	DPA2	X10-13a
X8-15	DPA1	X10-14a
X8-16	DPA0	X10-15a
X8-17	DPSN	X10-17a
X8-18	DPCP	X10-18a
X8-19	GND	ground
X8-20	GND	ground
X8-21	LDNM	X10-02b
X8-22	LDEC	X10-03b
X8-23	LDSA	X10-04b
X8-24	n.c.	
X8-25	SW3	X10-06b
X8-26	SW2	X10-07b
X8-27	SW1	X10-08b
X8-28	SW0	X10-09b
X8-29	SWACT/	X10-02c
X8-30	SWECM/	X10-03c
X8-31	GND	ground
X8-32	GND	ground
X8-33	RZPD/	X11-03a
X8-34	VMPD	X11-02a

Table 3-2: Connector X8

Connector X10 row a
(Red Interface)

pin	signal	connected to
X10-01a	GND	ground
X10-02a	FDDT	X8-06
X10-03a	FDCP	X8-05
X10-04a	FDRY/	X8-04
X10-05a	GND	ground
X10-06a	FDSL/	X8-03
X10-07a	FDCV	X8-02
X10-08a	DISX	n.c.(+)
X10-09a	DPA5	X8-11
X10-10a	DPA4	X8-12
X10-11a	GND	ground
X10-12a	DPA3	X8-13
X10-13a	DPA2	X8-14
X10-14a	DPA1	X8-15
X10-15a	DPA0	X8-16
X10-16a	GND	ground
X10-17a	DPSN	X8-17
X10-18a	DPCP	X8-18
X10-19a	FTPS	X8-09, -10
X10-20a	FTPS	X8-09, -10
X10-21a	GND	ground
X10-22a	RL4	X5-13
X10-23a	RL3	X5-14
X10-24a	RSG2	X5-11
X10-25a	SYNC2/	X5-12
X10-26a	RSG1	X5-09
X10-27a	GND	ground
X10-28a	RL5	X5-10
X10-29a	RL2	X5-07
X10-30a	RL1	X5-08
X10-31a	GND	ground
X10-32a	V+	voeding

Table 3-3: Connector X10, row a

Connector X10 row b
(Red Interface)

pin	signal	connected to
X10-01b	GND	ground
X10-02b	LDNM	X8-21
X10-03b	LDEC	X8-22
X10-04b	LDSA	X8-23
X10-05b	GND	ground
X10-06b	SW3	X8-25
X10-07b	SW2	X8-26
X10-08b	SW1	X8-27
X10-09b	SW0	X8-28
X10-10b	CPX	n.c.(+)
X10-11b	GND	ground
X10-12b	DI7	X11-12c, X15-12c, X18-12a
X10-13b	DI6	X11-13c, X15-13c, X18-13a
X10-14b	DI5	X11-14c, X15-14c, X18-14a
X10-15b	DI4	X11-15c, X15-15c, X18-15a
X10-16b	GND	ground
X10-17b	DO4	X11-17a, X15-17a
X10-18b	DO5	X11-18a, X15-18a
X10-19b	DO6	X11-19a, X15-19a
X10-20b	DO7	X11-20a, X15-20a
X10-21b	GND	ground
X10-22b	n.c.	
X10-23b	n.c.	
X10-24b	STSN/	X5-05
X10-25b	STBV/	X5-06
X10-26b	STNM/	X5-03
X10-27b	GND	ground
X10-28b	RCPT	X15-30a
X10-29b	RCPK	X19-28c
X10-30b	RCPA	X19-29c
X10-31b	GND	ground
X10-32b	V+	voeding

Table 3-4: Connector X10, row b

Connector X10 row c
(Red Interface)

pin	signal	connected to
X10-01c	GND	ground
X10-02c	SWACT/	X8-29
X10-03c	SWECM/	X8-30
X10-04c	n.c.	
X10-05c	GND	ground
X10-06c	ENX/	ground
X10-07c	RDSYN/	X11-07a
X10-08c	RDAB/	X11-08a
X10-09c	RDSW/	X11-09a
X10-10c	RDFD/	X11-10a
X10-11c	GND	ground
X10-12c	DI3	X11-12a, X14-12a, X15-12a
X10-13c	DI2	X11-13a, X14-13a, X15-13a
X10-14c	DI1	X11-14a, X14-14a, X15-14a
X10-15c	DI0	X11-15a, X14-15a, X15-15a
X10-16c	GND	ground
X10-17c	DO0	X11-17c, X12-28a, X15-17c, X16-28a
X10-18c	DO1	X11-18c, X14-18a, X15-18c, X18-18a
X10-19c	DO2	X11-19c, X15-19c
X10-20c	DO3	X11-20c, X15-20c
X10-21c	GND	ground
X10-22c	n.c.	
X10-23c	SDSP	X11-23a
X10-24c	STLD/	X11-24a
X10-25c	STEDA/	X11-25a, X14-24a, X18-24a
X10-26c	PRSTLD/	n.c.(+)
X10-27c	GND	ground
X10-28c	RDTT	X14-30a
X10-29c	RDTR	X18-30c
X10-30c	RCPR	X15-04c, X18-17c
X10-31c	GND	ground
X10-32c	V+	voeding

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Table 3-5: Connector X10, row c

Connector X11 row a
(Processor)

pin	signal	connected to
X11-01a	GND	ground
X11-02a	VMPD	X8-34
X11-03a	RZPD/	X8-33
X11-04a	RZNO	X5-04
X11-05a	GND	ground
X11-06a	IN6/	n.c.
X11-07a	RDSYN/	X10-07c
X11-08a	RDAB/	X10-08c
X11-09a	RDSW/	X10-09c
X11-10a	RDFD/	X10-10c
X11-11a	GND	ground
X11-12a	DI3	X10-12c, X14-12a, X15-12a
X11-13a	DI2	X10-13c, X14-13a, X15-13a
X11-14a	DI1	X10-14c, X14-14a, X15-14a
X11-15a	DI0	X10-15c, X14-15a, X15-15a
X11-16a	GND	ground
X11-17a	DO4	X10-17b, X15-17a
X11-18a	DO5	X10-18b, X15-18a
X11-19a	DO6	X10-19b, X15-19a
X11-20a	DO7	X10-20b, X15-20a
X11-21a	GND	ground
X11-22a	CPSYS	n.c.
X11-23a	SDSP	X10-23c
X11-24a	STLD/	X10-24c
X11-25a	STEDA/	X10-25c, X14-24a, X18-24a
X11-26a	GNPTR/	X15-10c
X11-27a	GND	ground
X11-28a	WAIT/	n.c.(+)
X11-29a	RST5.5	n.c.
X11-30a	SID	n.c.
X11-31a	GND	ground
X11-32a	V+	voeding

Table 3-6: Connector X11, row a

Connector X11 row c
(Processor)

pin	signal	connected to
X11-01c	GND	ground
X11-02c	REFX	n.c.(0)
X11-03c	PDX	n.c.
X11-04c	RSTX/	n.c.(+, open coll.)
X11-05c	GND	ground
X11-06c	ALEX	n.c.
X11-07c	S1X	n.c.
X11-08c	INTR	n.c.
X11-09c	PEST/	X15-10a
X11-10c	RDKG/	X14-10a, X18-10a
X11-11c	GND	ground
X11-12c	DI7	X10-12b, X15-12c, X18-12a
X11-13c	DI6	X10-13b, X15-13c, X18-13a
X11-14c	DI5	X10-14b, X15-14c, X18-14a
X11-15c	DI4	X10-15b, X15-15c, X18-15a
X11-16c	GND	ground
X11-17c	DO0	X10-17c, X12-28a, X15-17c, X16-28a
X11-18c	DO1	X10-18c, X14-18a, X15-18c, X18-18a
X11-19c	DO2	X10-19c, X15-19c
X11-20c	DO3	X10-20c, X15-20c
X11-21c	GND	ground
X11-22c	CVCP/	X14-22a, X18-22a
X11-23c	CVST	X14-23a, X18-23a
X11-24c	OUT2/	n.c.
X11-25c	SETPE/	X15-22c
X11-26c	PGALARM	X15-22a
X11-27c	GND	ground
X11-28c	STBI/	n.c.
X11-29c	LPRLB/	X19-09a
X11-30c	ALREL/	X19-10a
X11-31c	GND	ground
X11-32c	V+	voeding

Table 3-7: Connector X11, row c

Connector X12 row a
(Key generator I, wheels 1-4, Transmit)

pin	signal	connected to
X12-01a	GND	ground
X12-02a	EC1	X14-02a
X12-03a	ECV1	n.c.
X12-04a	ECV5	X13-03a
X12-05a	GND	ground
X12-06a	t14	X13-06a, X14-03a
X12-07a	VW2	n.c.
X12-08a	BSDLY	X13-08a, X14-09a
X12-09a	BS	X13-09a, X14-08a
X12-10a	SLIN	X14-30c
X12-11a	GND	ground
X12-12a	LB0	X15-23a
X12-13a	LB4	X13-12a
X12-14a	n.c.	
X12-15a	n.c.	
X12-16a	GND	ground
X12-17a	n.c.	
X12-18a	n.c.	
X12-19a	n.c.	
X12-20a	CRYPTO/	X12-20c, X13-20a, X14-06c
X12-21a	GND	ground
X12-22a	LBEN1/	ground
X12-23a	n.c.	
X12-24a	CPES	X13-24a, X14-03c
X12-25a	ES13	n.c.
X12-26a	DSLDIS/	n.c.(+)
X12-27a	GND	ground
X12-28a	DSL1	X10-17c, X11-17c, X15-17c, X16-28a
X12-29a	CPDSL	X13-29a, X14-26a
X12-30a	DSLOVN	X13-30a, X14-25a
X12-31a	GND	ground
X12-32a	V+	voeding

Table 3-8: Connector X12, row a

Connector X12 row c
(Key generator I, wheels 1-4, Transmit)

pin	signal	connected to
X12-01c	GND	ground
X12-02c	t24	X13-02c, X14-04c
X12-03c	PT4	X13-10a
X12-04c	PTEN	X13-04c, X14-07a
X12-05c	GND	ground
X12-06c	t24/	X13-06c, X14-04a
X12-07c	VW6	X13-07a
X12-08c	WIELRES	X13-08c, X14-07c
X12-09c	VW10	X13-09c, X14-08c
X12-10c	CRSTS	X13-10c, X14-10c
X12-11c	GND	ground
X12-12c	LB1	X14-22c
X12-13c	LB5	X13-12c
X12-14c	n.c.	
X12-15c	n.c.	
X12-16c	GND	ground
X12-17c	n.c.	
X12-18c	n.c.	
X12-19c	n.c.	
X12-20c	PTINEN/	X12-20a, X13-20a, X14-06c
X12-21c	GND	ground
X12-22c	LBEN2/	ground
X12-23c	n.c.	
X12-24c	CRSTS/	X13-24c, X14-09c
X12-25c	ES53	X13-25a
X12-26c	n.c.	
X12-27c	GND	ground
X12-28c	DSL2	X13-28a
X12-29c	DSCH1	n.c.(+)
X12-30c	DSCH2	X13-29c
X12-31c	GND	ground
X12-32c	V+	voeding

Table 3-9: Connector X12, row c

Connector X13 row a
(Key generator I, wheels 5-8, Transmit)

pin	signal	connected to
X13-01a	GND	ground
X13-02a	EC1	X14-23c
X13-03a	ECV1	X12-04a
X13-04a	ECV5	X14-02c
X13-05a	GND	ground
X13-06a	t14	X12-06a, X14-03a
X13-07a	VW2	X12-07c
X13-08a	BSDLY	X12-08a, X14-09a
X13-09a	BS	X12-09a, X14-08a
X13-10a	SLIN	X12-03c
X13-11a	GND	ground
X13-12a	LB0	X12-13a
X13-13a	LB4	X14-26c
X13-14a	n.c.	
X13-15a	n.c.	
X13-16a	GND	ground
X13-17a	n.c.	
X13-18a	n.c.	
X13-19a	n.c.	
X13-20a	CRYPTO/	X12-20a, -20c, X14-06c
X13-21a	GND	ground
X13-22a	LBEN1/	ground
X13-23a	n.c.	
X13-24a	CPES	X12-24a, X14-03c
X13-25a	ES13	X12-25c
X13-26a	DSLDIS/	n.c.(+)
X13-27a	GND	ground
X13-28a	DSL1	X12-28c
X13-29a	CPDSL	X12-29a, X14-26a
X13-30a	DSLOVN	X12-30a, X14-25a
X13-31a	GND	ground
X13-32a	V+	voeding

Table 3-10: Connector X13, row a

Connector X13 row c
(Key generator I, wheels 5-8, Transmit)

pin	signal	connected to
X13-01c	GND	ground
X13-02c	t24	X12-02c, X14-04c
X13-03c	PT4	X14-06a
X13-04c	PTEN	X12-04c, X14-07a
X13-05c	GND	ground
X13-06c	t24/	X12-06c, X14-04a
X13-07c	VW6	n.c.(+)
X13-08c	WIELRES	X12-08c, X14-07c
X13-09c	VW10	X12-09c, X14-08c
X13-10c	CRSTS	X12-10c, X14-10c
X13-11c	GND	ground
X13-12c	LB1	X12-13c
X13-13c	LB5	X14-28c
X13-14c	n.c.	
X13-15c	n.c.	
X13-16c	GND	ground
X13-17c	n.c.	
X13-18c	n.c.	
X13-19c	n.c.	
X13-20c	PTINEN/	ground
X13-21c	GND	ground
X13-22c	LBEN2/	ground
X13-23c	n.c.	
X13-24c	CRSTS/	X12-24c, X14-09c
X13-25c	ES53	X14-24c
X13-26c	n.c.	
X13-27c	GND	ground
X13-28c	DSL2	X14-12c
X13-29c	DSCH1	X12-30c
X13-30c	DSCH2	X14-25c
X13-31c	GND	ground
X13-32c	V+	voeding

Table 3-11: Connector X13, row c

Connector X14 row a
(Key generator II, wheel 9, control, ECCM, Transmit)

pin	signal	connected to
X14-01a	GND	ground
X14-02a	EC1	X12-02a
X14-03a	t14	X12-06a, X13-06a
X14-04a	t24/	X12-06c, X13-06c
X14-05a	GND	ground
X14-06a	PT8	X13-03c
X14-07a	PTEN	X12-04c, X13-04c
X14-08a	BSDLY	X12-09a, X13-09a
X14-09a	BS	X12-08a, X13-08a
X14-10a	RDKG/	X11-10c, X18-10a
X14-11a	GND	ground
X14-12a	DI37	X10-12c, X11-12a, X15-12a
X14-13a	DI26	X10-13c, X11-13a, X15-13a
X14-14a	DI15	X10-14c, X11-14a, X15-14a
X14-15a	DI04	X10-15c, X11-15a, X15-15a
X14-16a	GND	ground
X14-17a	REC/	n.c.(+)
X14-18a	DO1	X10-18c, X11-18c, X15-18c, X18-18a
X14-19a	RESBEST/	n.c.(+)
X14-20a	n.c.	
X14-21a	GND	ground
X14-22a	CVCP/	X11-22c, X18-22a
X14-23a	CVST	X11-23c, X18-23a
X14-24a	STEDA/	X10-25c, X11-25a, X18-24a
X14-25a	DSLOVN	X12-30a, X13-30a
X14-26a	CPDSL	X12-29a, X13-29a
X14-27a	GND	ground
X14-28a	CPCR	X15-26a, X18-28a
X14-29a	SLUIT	X15-28a
X14-30a	ECMIN	X10-28c
X14-31a	GND	ground
X14-32a	V+	voeding

Table 3-12: Connector X14, row a

Connector X14 row c
(Key generator II, wheel 9, control, ECCM, Transmit)

pin	signal	connected to
X14-01c	GND	ground
X14-02c	ECV9	X13-04a
X14-03c	CPES	X12-24a, X13-24a
X14-04c	t24	X12-02c, X13-02c
X14-05c	GND	ground
X14-06c	CRYPTO/	X12-20a, X13-20a
X14-07c	WIELRES	X12-08c, X13-08c
X14-08c	VW10	X12-09c, X13-09c
X14-09c	CRSTS/	X12-24c, X13-24c
X14-10c	CRSTS	X12-10c, X13-10c
X14-11c	GND	ground
X14-12c	DSL3	X13-28c
X14-13c	OPVB/	X15-25c
X14-14c	ECCMR/	X15-03a, X18-14c
X14-15c	ECCMT/	X15-25a, X18-15c
X14-16c	GND	ground
X14-17c	CPD	X15-29a
X14-18c	SGSTEN/	X15-23c
X14-19c	BSA/	X15-24a
X14-20c	CRSTA/	X15-24c
X14-21c	GND	ground
X14-22c	LB1	X12-12c
X14-23c	EC5	X13-02a
X14-24c	ES93	X13-25c
X14-25c	DSCH3	X13-30c
X14-26c	LB8	X13-13a
X14-27c	GND	ground
X14-28c	LB9	X13-13c
X14-29c	MIXIN	n.c.(+)
X14-30c	ECMUIT	X12-10a
X14-31c	GND	ground
X14-32c	V+	voeding

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Table 3-13: Connector X14, row c

Connector X15 row a
(Pattern unit)

pin	signal	connected to
X15-01a	GND	ground
X15-02a	BCPR	X19-04a
X15-03a	ECCMR/	X14-14c, X18-14c
X15-04a	LBOR	X16-12a
X15-05a	GND	ground
X15-06a	SGSTENR/	X18-18c
X15-07a	PHEN/	ground
X15-08a	PGEN/	ground
X15-09a	OSCDIS/	n.c.
X15-10a	PEST/	X11-09c
X15-11a	GND	ground
X15-12a	DI3	X10-12c, X11-12a, X14-12a
X15-13a	DI2	X10-13c, X11-13a, X14-13a
X15-14a	DI1	X10-14c, X11-14a, X14-14a
X15-15a	DI0	X10-15c, X11-15a, X14-15a
X15-16a	GND	ground
X15-17a	DO4	X10-17b, X11-17a
X15-18a	DO5	X10-18b, X11-18a
X15-19a	DO6	X10-19b, X11-19a
X15-20a	DO7	X10-20b, X11-20a
X15-21a	GND	ground
X15-22a	PGALARM	X11-26c
X15-23a	LBOT	X12-12a
X15-24a	BSAT/	X14-19c
X15-25a	ECCMT/	X14-15c, X18-15c
X15-26a	CPCR	X14-28a, X18-28a
X15-27a	GND	ground
X15-28a	SLUITT	X14-29a
X15-29a	CPDT	X14-17c
X15-30a	RCPT	X10-28b
X15-31a	GND	ground
X15-32a	V+	voeding

Table 3-14: Connector X15, row a

Connector X15 row c
(Pattern unit)

pin	signal	connected to
X15-01c	GND	ground
X15-02c	BDTR	X19-03a
X15-03c	BDTSG	X18-29c
X15-04c	CPDR	X10-30c, X18-17c
X15-05c	GND	ground
X15-06c	CRSTAR	X18-20c
X15-07c	BSAR/	X18-19c
X15-08c	OPVBR	X18-13c
X15-09c	CRYPTOR/	n.c.
X15-10c	GNPTNR/	X11-26a
X15-11c	GND	ground
X15-12c	DI7	X10-12b, X11-12c, X18-12a
X15-13c	DI6	X10-13b, X11-13c, X18-13a
X15-14c	DI5	X10-14b, X11-14c, X18-14a
X15-15c	DI4	X10-15b, X11-15c, X18-15a
X15-16c	GND	ground
X15-17c	DO0	X10-17c, X11-17c, X12-28a, X16-28a
X15-18c	DO1	X10-18c, X11-18c, X14-18a, X18-18a
X15-19c	DO2	X10-19c, X11-19c
X15-20c	DO3	X10-20c, X11-20c
X15-21c	GND	ground
X15-22c	SETPE/	X11-25c
X15-23c	SGSTENT/	X14-18c
X15-24c	CRSTAT	X14-20c
X15-25c	OPVBT/	X14-13c
X15-26c	ALX	ground
X15-27c	GND	ground
X15-28c	BDTT	X19-17a
X15-29c	BDTT/	X19-18a
X15-30c	PGALBI/	X19-08a
X15-31c	GND	ground
X15-32c	V+	voeding

Table 3-15: Connector X15, row c

Connector X16 row a
(Key generator I, wheels 1-4, Receiver)

pin	signal	connected to
X16-01a	GND	ground
X16-02a	EC1	X18-02a
X16-03a	ECV1	n.c.
X16-04a	ECV5	X17-03a
X16-05a	GND	ground
X16-06a	t14	X17-06a, X18-03a
X16-07a	VW2	n.c.
X16-08a	BSDLY	X17-08a, X18-09a
X16-09a	BS	X17-09a, X18-08a
X16-10a	SLIN	X16-26a
X16-11a	GND	ground
X16-12a	LB0	X15-04a
X16-13a	LB4	X17-12a
X16-14a	n.c.	
X16-15a	n.c.	
X16-16a	GND	ground
X16-17a	n.c.	
X16-18a	n.c.	
X16-19a	n.c.	
X16-20a	CRYPTO/	X16-20c, X17-20a, X18-06c
X16-21a	GND	ground
X16-22a	LBEN1/	ground
X16-23a	n.c.	
X16-24a	CPES	X17-24a, X18-03c
X16-25a	ES13	n.c.
X16-26a	DSLDIS/	X16-10a, [n.c.(+)
X16-27a	GND	ground
X16-28a	DSL1	X10-17c, X11-17c, X15-17c, X12-28a
X16-29a	CPDSL	X17-29a, X18-26a
X16-30a	DSLOVN	X17-30a, X18-25a
X16-31a	GND	ground
X16-32a	V+	voeding

Table 3-16: Connector X16, row a

Connector X16 row c
(Key generator I, wheels 1-4, Receiver)

pin	signal	connected to
X16-01c	GND	ground
X16-02c	t24	X17-02c, X18-04c
X16-03c	PT4	X17-10a
X16-04c	PTEN	X17-04c, X18-07a
X16-05c	GND	ground
X16-06c	t24/	X17-06c, X18-04a
X16-07c	VW6	X17-07a
X16-08c	WIELRES	X17-08c, X18-07c
X16-09c	VW10	X17-09c, X18-08c
X16-10c	CRSTS	X17-10c, X18-10c
X16-11c	GND	ground
X16-12c	LB1	X18-22c
X16-13c	LB5	X17-12c
X16-14c	n.c.	
X16-15c	n.c.	
X16-16c	GND	ground
X16-17c	n.c.	
X16-18c	n.c.	
X16-19c	n.c.	
X16-20c	PTINEN/	X16-20a, X17-20a, X18-06c
X16-21c	GND	ground
X16-22c	LBEN2/	ground
X16-23c	n.c.	
X16-24c	CRSTS/	X17-24c, X18-09c
X16-25c	ES53	X17-25a
X16-26c	n.c.	
X16-27c	GND	ground
X16-28c	DSL2	X17-28a
X16-29c	DSCH1	n.c.(+)
X16-30c	DSCH2	X17-29c
X16-31c	GND	ground
X16-32c	V+	voeding

Table 3-17: Connector X16, row c

Connector X17 row a
(Key generator I, wheels 5-8, Receiver)

pin	signal	connected to
X17-01a	GND	ground
X17-02a	EC1	X18-23c
X17-03a	ECV1	X16-04a
X17-04a	ECV5	X18-02c
X17-05a	GND	ground
X17-06a	t14	X16-06a, X18-03a
X17-07a	VW2	X16-07c
X17-08a	BSDLY	X16-08a, X18-09a
X17-09a	BS	X16-09a, X18-08a
X17-10a	SLIN	X16-03c
X17-11a	GND	ground
X17-12a	LB0	X16-13a
X17-13a	LB4	X18-26c
X17-14a	n.c.	
X17-15a	n.c.	
X17-16a	GND	ground
X17-17a	n.c.	
X17-18a	n.c.	
X17-19a	n.c.	
X17-20a	CRYPTO/	X16-20a, X16-20c, X18-06c
X17-21a	GND	ground
X17-22a	LBEN1/	ground
X17-23a	n.c.	
X17-24a	CPES	X16-24a, X18-03c
X17-25a	ES13	X16-25c
X17-26a	DSLDIS/	n.c.(+)
X17-27a	GND	ground
X17-28a	DSL1	X16-28c
X17-29a	CPDSL	X16-29a, X18-26a
X17-30a	DSLOVN	X16-30a, X18-25a
X17-31a	GND	ground
X17-32a	V+	voeding

Table 3-18: Connector X17, row a

Connector X17 row c
(Key generator I, wheels 5-8, Receiver)

pin	signal	connected to
X17-01c	GND	ground
X17-02c	t24	X16-02c, X18-04c
X17-03c	PT4	X18-06a
X17-04c	PTEN	X16-04c, X18-07a
X17-05c	GND	ground
X17-06c	t24/	X16-06c, X18-04a
X17-07c	VW6	n.c.(+)
X17-08c	WIELRES	X16-08c, X18-07c
X17-09c	VW10	X16-09c, X18-08c
X17-10c	CRSTS	X16-10c, X18-10c
X17-11c	GND	ground
X17-12c	LB1	X16-13c
X17-13c	LB5	X18-28c
X17-14c	n.c.	
X17-15c	n.c.	
X17-16c	GND	ground
X17-17c	n.c.	
X17-18c	n.c.	
X17-19c	n.c.	
X17-20c	PTINEN/	ground
X17-21c	GND	ground
X17-22c	LBEN2/	ground
X17-23c	n.c.	
X17-24c	CRSTS/	X16-24c, X18-09c
X17-25c	ES53	X18-24c
X17-26c	n.c.	
X17-27c	GND	ground
X17-28c	DSL2	X18-12c
X17-29c	DSCH1	X16-30c
X17-30c	DSCH2	X18-25c
X17-31c	GND	ground
X17-32c	V+	voeding

Table 3-19: Connector X17, row c

Connector X18 row a
(Key generator II, wheel 9, control, ECCM, Receiver)

pin	signal	connected to
X18-01a	GND	ground
X18-02a	EC1	X16-02a
X18-03a	t14	X16-06a, X17-06a
X18-04a	t24/	X16-06c, X17-06c
X18-05a	GND	ground
X18-06a	PT8	X17-03c
X18-07a	PTEN	X16-04c, X17-04c
X18-08a	BSDLY	X16-09a, X17-09a
X18-09a	BS	X16-08a, X17-08a
X18-10a	RDKG/	X11-10c, X14-10a
X18-11a	GND	ground
X18-12a	DI37	X10-12b, X11-12c, X15-12c
X18-13a	DI26	X10-13b, X11-13c, X15-13c
X18-14a	DI15	X10-14b, X11-14c, X15-14c
X18-15a	DI04	X10-15b, X11-15c, X15-15c
X18-16a	GND	ground
X18-17a	REC/	ground
X18-18a	DO1	X10-18c, X11-18c, X14-18a, X15-18c
X18-19a	RESBEST/	n.c.(+)
X18-20a	n.c.	
X18-21a	GND	ground
X18-22a	CVCP/	X11-22c, X14-22a
X18-23a	CVST	X11-23c, X14-23a
X18-24a	STEDA/	X10-25c, X11-25a, X14-24a
X18-25a	DSLOVN	X16-30a, X17-30a
X18-26a	CPDSL	X16-29a, X17-29a
X18-27a	GND	ground
X18-28a	CPCR	X14-28a, X15-26a
X18-29a	SLUIT	X18-30a
X18-30a	ECMIN	X18-29a
X18-31a	GND	ground
X18-32a	V+	voeding

Table 3-20: Connector X18, row a

Connector X18 row c
(Key generator II, wheel 9, control, ECCM, Receiver)

pin	signal	connected to
X18-01c	GND	ground
X18-02c	ECV9	X17-04a
X18-03c	CPES	X16-24a, X17-24a
X18-04c	t24	X16-02c, X17-02c
X18-05c	GND	ground
X18-06c	CRYPTO/	X16-20a, X16-20c, X17-20a
X18-07c	WIELRES	X16-08c, X17-08c
X18-08c	VW10	X16-09c, X17-09c
X18-09c	CRSTS/	X16-24c, X17-24c
X18-10c	CRSTS	X16-10c, X17-10c
X18-11c	GND	ground
X18-12c	DSL3	X17-28c
X18-13c	OPVB/	X15-08c
X18-14c	ECCMR/	X14-14c, X15-03a
X18-15c	ECCMT/	X14-15c, X15-25a
X18-16c	GND	ground
X18-17c	CPD	X10-30c, X15-04c
X18-18c	SGSTEN/	X15-06a
X18-19c	BSA/	X15-07c
X18-20c	CRSTA/	X15-06c
X18-21c	GND	ground
X18-22c	LB1	X16-12c
X18-23c	EC5	X17-02a
X18-24c	ES93	X17-25c
X18-25c	DSCH3	X17-30c
X18-26c	LB8	X17-13a
X18-27c	GND	ground
X18-28c	LB9	X17-13c
X18-29c	MIXIN	X15-03c
X18-30c	ECMUIT	X10-29c
X18-31c	GND	ground
X18-32c	V+	voeding

Table 3-21: Connector X18, row c

Connector X19 row a
(Black Interface)

pin	signal	connected to
X19-01a	GND	ground
X19-02a	n.c.	
X19-03a	BDTR	X15-02c
X19-04a	BCPR	X15-02a
X19-05a	GND	ground
X19-06a	n.c.	
X19-07a	n.c.	
X19-08a	PGALBI/	X15-30c
X19-09a	LPRLB/	X11-29c
X19-10a	ALREL/	X11-30c
X19-11a	GND	ground
X19-12a	BL1	X3-10
X19-13a	n.c.	
X19-14a	n.c.	
X19-15a	n.c.	
X19-16a	GND	ground
X19-17a	BDTT	X15-28c
X19-18a	BDTT/	X15-29c
X19-19a	GND	ground
X19-20a	LASO	X5-01
X19-21a	GND	ground
X19-22a	n.c.	
X19-23a	n.c.	
X19-24a	n.c.	
X19-25a	n.c.	
X19-26a	n.c.	
X19-27a	GND	ground
X19-28a	n.c.	
X19-29a	n.c.	
X19-30a	n.c.	
X19-31a	GND	ground
X19-32a	VB	X3-01, -02

Table 3-22: Connector X19, row a

Connector X19 row c
(Black Interface)

pin	signal	connected to
X19-01c	GND	ground
X19-02c	BL3	X3-15
X19-03c	BL4	X3-16
X19-04c	BSG1	X3-13
X19-05c	GND	ground
X19-06c	ALNO	X3-06
X19-07c	ALNC	X3-07
X19-08c	ALC	X3-05
X19-09c	n.c.	
X19-10c	VRC	n.c.
X19-11c	GND	ground
X19-12c	n.c.	
X19-13c	BL2	X3-11
X19-14c	BSG2	X3-12
X19-15c	BSC	X3-14
X19-16c	GND	ground
X19-17c	GND	ground
X19-18c	GND	ground
X19-19c	LASE	X3-03
X19-20c	LASC	X3-04
X19-21c	GND	ground
X19-22c	n.c.	
X19-23c	RFCUIT	n.c.
X19-24c	RFCIN	X19-25c
X19-25c	RFCUIT/	X19-24c
X19-26c	n.c.	
X19-27c	GND	ground
X19-28c	RCPK	X10-29b
X19-29c	RCPA	X10-30b
X19-30c	GND	ground
X19-31c	GND	ground
X19-32c	VB	X3-01, -02

Table 3-23: Connector X19, row c

STATUS (OPERATIONAL STATE + MODE) / EFFECT OF:	:1	1A	1AD	1ADF	1ADG	1ADFG	1AF	1AG	1AFG	1D	1DF	1DG	1DFG	1F	1G	1FG
1 SWITCHING ON	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG
2 RED SIGNAL CONNECTOR																
2.1 Sync command	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2.2 Remote zeroize	1	1A	1AD	1ADF	1ADG	1ADFG	1AF	1AG	1AFG	1D	1DF	1DG	1DFG	1F	1G	1FG
3 BLACK SIGNAL CONNECTOR																
3.1 Attention-word	1	-	-	-	-	-	-	-	-	1D	1DF	1DG	1DFG	1F	1G	1FG
3.2 Change crypto var.	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3.3 Crypto start (ECCM off)	1	-	-	-	-	-	-	-	-	-	-	1D	1DF	-	1	1F
3.4 Crypto start (ECCM on)	1G	-	-	-	-	-	-	-	-	1DG	1DFG	-	-	1FG	-	-
3.5 Compromise	1D	-	-	-	-	-	-	-	-	1D	1DF	1DG	1DFG	1FD	1GD	1FGD
3.6 Rest	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
4 EFFECT ON OPERATION																
4.1 Transport/sleutel uit	2	1A	1AD	1ADF	1ADG	1ADFG	1AF	1AG	1AFG	2	2F	2G	2FG	2F	2G	2FG
4.2 Lamp test	1									1	1F	1G	1FG	1F	1G	1FG
4.3 Test alarm reset	1A	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1A	1AF	1AG	1AFG	1AF	1AG	1AFG
4.4 Test toestel	3B	-	-	-	-	-	-	-	-	3B	3BGF	3B	3BFG	3BFG	3B	3BFG
4.5 Base key	3B	-	-	-	-	-	-	-	-	3B	3BF	3BG	3BFG	3BF	3BG	3BFG
4.6 Sleutel laden (Load crypto)	5	-	-	-	-	-	-	-	-	5	5F	5G	5FG	5F	5G	5FG
4.7 Change crypto		-	-	-	-	-	-	-	-	1	1F	1G	1FG	-	-	-
4.8 Load spare crypto	5	-	-	-	-	-	-	-	-	5	5F	5G	5FG	5F	5G	5FG
4.9 LA Loop	1	-	-	-	-	-	-	-	-	1	1F	1G	1FG	1F	1G	1FG
4.10 Bedrijf (Operation)		-	-	-	-	-	-	-	-	1	1F	1G	1FG	-	-	-
4.11 Onderhoud 1	1	-	-	-	-	-	-	-	-	1	1F	1G	1FG	1F	1G	1FG
4.12 Onderhoud 2 (Maintenance)	3BFG	-	-	-	-	-	-	-	-	3BFG	3BFG	3BFG	3BFG	3BFG	3BFG	3BFG
4.13 ECCM switch on	1F	-	-	-	-	-	-	-	-	1DF	-	1DFG	-	-	1FG	-
4.14 ECCM switch off	-	-	-	-	-	-	-	-	-	-	1D	-	1DG	1	-	1G
5 ALARM	1A	-	-	-	-	-	-	-	-	1A	1AF	1AG	1AFG	1AF	1AG	1AFG

Note: To change of mode from mode C or E, turn the function selector switch.
* Means: Combination is not possible

Table 4-1: Status and changes of status in operational state 1

STATUS (OPERATIONAL STATE + MODE)	2	2D	2DG	2DF	2DFG	2F	2FG	2G
EFFECT OF:								
1 SWITCHING ON	1FG	1FG	1FG	1FG	1FG	1FG	1FG	1FG
2 RED SIGNAL CONNECTOR								
2.1 Sync command	-	-	-	-	-	-	-	-
2.2 Remote zeroize	-	-	-	-	-	-	-	-
3 BLACK SIGNAL CONNECTOR								
3.1 Attention-word	2	2D	2DG	2DF	2DFG	2F	2FG	2G
3.2 Change crypto var.	-	-	-	-	-	-	-	-
3.3 Crypto start (ECCM off)	-	-	2D	-	2DF	-	2F	2
3.4 Crypto start (ECCM on)	2G	2DG	-	2DFG	-	2FG	-	-
3.5 Compromise	2D	-	-	-	-	2DF	2DFG	2DG
3.6 Rest	-	-	-	-	-	-	-	-
4 EFFECT ON OPERATION								
4.1 Transport/sleutel uit	-	2	2G	2F	2FG	-	-	-
4.2 Lamp test	-	2	2G	2F	2FG	-	-	-
4.3 Test alarm reset	-	2	2G	2F	2FG	-	-	-
4.4 Test toestel	-	2	2G	2F	2FG	-	-	-
4.5 Base key	-	2	2G	2F	2FG	-	-	-
4.6 Sleutel laden (Load crypto)	-	2	2G	2F	2FG	-	-	-
4.7 Change crypto	-	2	2G	2F	2FG	-	-	-
4.8 Load spare crypto	-	2	2G	2F	2FG	-	-	-
4.9 LA Loop	-	2	2G	2F	2FG	-	-	-
4.10 Bedrijf (Operation)	-	2	2G	2F	2FG	-	-	-
4.11 Onderhoud 1	-	2	2G	2F	2FG	-	-	-
4.12 Onderhoud 2 (Maintenance)	-	2	2G	2F	2FG	-	-	-
4.13 ECCM switch on	-	-	-	-	-	-	-	-
4.14 ECCM switch off	-	-	-	-	-	-	-	-
5 ALARM	1A	1AD	1ADG	1ADF	1ADFG	1AF	1AG	1AG

Table 4-2: Status and changes of status in operational state 2

STATUS (OPERATIONAL STATE + MODE)	3	3A	3AFG	3B	3BD	3BDG	3BDF	3BDFG	3BG	3BF	3BFG	3D	3DF	3DG	3DFG	3G	3F	3FG
EFFECT OF:																		
1 SWITCHING ON	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG	3FG
2 RED SIGNAL CONNECTOR																		
2.1 Sync command	3	-	-	3B	3BD	3BDG	3BDF	3BDFG	3BG	3BF	3BFG	3D	3DF	3DG	3DFG	3G	3F	3FG
2.2 Remote zeroize	1	1A	1AFG	1	1D	1DG	1DF	1DFG	1G	1F	1FG	1D	1DF	1DG	1DFG	1G	1F	1FG
3 BLACK SIGNAL CONNECTOR																		
3.1 Attention-word	3	-	-	3	3D	3DG	3DF	3DFG	3G	3F	3FG	3D	3DF	3DG	3DFG	3G	3F	3FG
3.2 Change crypto var.	-	-	-	*	*	*	*	*	*	*	*	-	-	-	-	-	-	-
3.3 Crypto start(ECCM off)	3B	-	-	*	*	*	*	*	*	*	*	3BD	3BDF	3BD	3BDF	3B	3BF	3BF
3.4 Crypto start(ECCM on)	3BG	-	-	*	*	*	*	*	*	*	*	3BDG	3BDFG	3BDFG	3BDFG	3BG	3BFG	3BFG
3.5 Compromise	3D	-	-	*	*	*	*	*	*	*	*	3D	3DF	3DG	3DFG	3DG	3DF	3DFG
3.6 Rest	3B	-	-	*	*	*	*	*	*	*	*	3BD	3BF	3BDG	3BDFG	3BG	3BF	3BFG
4 EFFECT ON OPERATION																		
4.1 Transport/sleutel uit	1	1A	1AFG	1	1	1G	1F	1FG	1G	1F	1FG	1	1F	1G	1FG	1G	1F	1FG
4.2 Lamp test	3	-	-	3B	3B	3BG	3BF	3BFG	3BG	3BF	3BFG	3	3F	3G	3FG	3G	3F	3FG
4.3 Test alarm reset	3A	3FG	3FG	3A	3AD	3AG	3AF	3AFG	3AG	3AF	3AFG	3A	3AF	3AG	3AFG	3AG	3AF	3AF
4.4 Test toestel	3B	-	-	3B	3B	3B	3BFG	3BFG	3B	3BFG	3BFG	3B	3BFG	3B	3BFG	3B	3BFG	3BFG
4.5 Base key	3B	-	-	3B	3B	3BG	3BF	3BFG	3BG	3BF	3BFG	3B	3BF	3BG	3BFG	3BG	3BF	3BFG
4.6 Sleutel laden	4	-	-	4B	4B	4BG	4BF	4BFG	4BG	4BF	4BFG	4	4F	4G	4FG	4G	4F	4FG
4.7 Change crypto	-	-	-	-	3B	3BG	3BF	3BFG	-	-	-	3	3F	3G	3FG	-	-	-
4.8 Load spare crypto	4	-	-	4B	4B	4BG	4BF	4BFG	4BG	4BF	4BFG	4	4F	4G	4FG	4G	4F	4FG
4.9 LA Loop	3	-	-	3B	3B	3BG	3BF	3BFG	3BG	3BF	3BFG	3	3F	3G	3FG	3G	3F	3FG
4.10 Bedrijf (Operation)	-	-	-	-	3B	3BG	3BF	3BFG	-	-	-	3	3F	3G	3FG	-	-	-
4.11 Onderhoud 1	3	-	-	3B	3B	3BG	3BF	3BFG	3BG	3BF	3BFG	3	3F	3G	3FG	3G	3F	3FG
4.12 Onderhoud 2	3BFG	-	-	3BFG	3BFG	3BFG	3BFG	3BFG	3BFG	3BFG	3BFG	3BGF	3BFG	3BFG	3BFG	3BFG	3BFG	3BFG
4.13 ECCM switch on	3F	-	-	3BF	3BDF	3BDFG	-	-	3BFG	-	-	3DF	-	3FG	-	3FG	-	-
4.14 ECCM switch off	-	-	-	-	-	-	3BD	3BDG	-	3B	3BG	-	3D	-	3DG	-	3	3G
5 ALARM	3A	-	-	3A	3AD	3ADG	3ADF	3ADFG	3AG	3AF	3AFG	3AD	3ADF	3ADG	3ADFG	3AG	3AF	3AFG

Table 4-3: Status and changes of status in operational state 3

STATUS (OPERATIONAL STATE + MODE):	4	4A	4AFG	4B	4BD	4BDG	4BDF	4BDFG	4BG	4BF	4BFG	4D	4DF	4DG	4DFG	4G	4F	4FG
EFFECT OF:																		
1 SWITCHING ON	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG	4FG
2 RED SIGNAL CONNECTOR																		
2.1 Sync command	4	-		4B	4BD	4BDG	4BDF	4BDFG	4BG	4BF	4BFG	4D	4DF	4DG	4DFG	4G	4F	4FG
2.2 Remote zeroize	1	1	1AFG	1	1D	1DG	1DF	1DFG	1G	1F	1FG	1D	1DF	1DG	1DFG	1G	1F	1FG
3 BLACK SIGNAL CONNECTOR																		
3.1 Attention-word	4	-	-	4	4D	4DG	4DF	4DFG	4G	4F	4FG	4D	4DF	4DG	4DFG	4G	4F	4FG
3.2 Change crypto var.	6	-	-	*	*	*	*	*	*	*	*	6D	6DF	6DG	6DFG	6G	6F	6FG
3.3 Crypto start(ECCM off)	4B	-	-	*	*	*	*	*	*	*	*	4BD	4BDF	4BD	4BDF	4B	4BF	4BF
3.4 Crypto start(ECCM on)	4BG	-	-	*	*	*	*	*	*	*	*	4BDG	4BDFG	4BDG	4BDFG	4BG	4BFG	4BFG
3.5 Compromise	4D	-	-	*	*	*	*	*	*	*	*	4D	4DF	4DG	4BFG	4DG	4DF	4DFG
3.6 Rest	4B	-	-	*	*	*	*	*	*	*	*	4BD	4BDF	4BDG	4BDFG	4BG	4BF	4BFG
4 EFFECT ON OPERATION																		
4.1 Transport/sleutel uit	1	1A	1AFG	1	1	1G	1F	1FG	1G	1F	1FG	1	1F	1G	1FG	1G	1F	1FG
4.2 Lamp test	4	-	-	4B	4B	4BG	4BF	4BFG	4BG	4BF	4BFG	4	4F	4G	4FG	4G	4F	4FG
4.3 Test alarm reset	4A	4FG	4FG	4A	4A	4AG	4AF	4AFG	4AG	4AF	4AFG	4A	4AF	4AG	4AFG	4AG	4AF	4AFG
4.4 Test toestel	4B	-	-	4B	4B	4B	4BFG	4BFG	4B	4BFG	4BFG	4B	4BFG	4B	4BFG	4	4BFG	4BFG
4.5 Base key	4B	-	-	4B	4B	4BG	4BF	4BFG	4BG	4BF	4BFG	4B	4BF	4B	4BFG	4BG	4BF	4BFG
4.6 Sleutel laden	4	-	-	4B	4B	4BG	4BF	4BFG	4BG	4BF	4BFG	4	4F	4G	4FG	4G	4F	4FG
4.7 Change crypto	6E	-	-	6E	6E	6E	6EF	6EFG	6EG	6EF	6EFG	6E	6EF	6EG	6EFG	6EG	6EF	6EFG
4.8 Load spare crypto	4	-	-	4B	4B	4BG	4BF	4BFG	4BG	4BF	4BFG	4	4F	4G	4FG	4G	4F	4FG
4.9 LA Loop	4	-	-	4B	4B	4BG	4BF	4BFG	4BG	4BF	4BFG	4	4F	4G	4FG	4G	4F	4FG
4.10 Bedrijf (Operation)	-	-	-	-	4B	4BG	4BF	4BFG	-	-	-	4	4F	4G	4FG	-	-	-
4.11 Onderhoud 1	4	-	-	4B	4B	4BG	4BF	4BFG	4BG	4BF	4BFG	4	4F	4G	4FG	4G	4F	4FG
4.12 Onderhoud 2	4BFG	-	-	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG
4.13 ECCM switch on	4F	-	-	4BF	4BDF	4BDFG	-	-	4BFG	-	-	4DF	-	4BFG	-	4BFG	-	-
4.14 ECCM switch off	-	-	-	-	-	-	4BD	4BDG	-	4B	4BG	-	4D	-	4DG	-	4	4G
5 ALARM	4A	-	-	4A	4AD	4ADG	4ADF	4ADFG	4AG	4AF	4AFG	4AD	4ADF	4ADG	4ADFG	4AG	4AF	4AFG

Table 4-4: Status and changes of status in operational state 4

STATUS (OPERATIONAL STATE + MODE):	5	5A	5AFG	5D	5DF	5DG	5DFG	5G	5F	5FG
EFFECT OF:										
1 SWITCHING ON	5FG	5FG	5FG	5FG	5FG	5FG	5FG	5FG	5FG	5FG
2 RED SIGNAL CONNECTOR										
2.1 Sync command	-	-	-	-	-	-	-	-	-	-
2.2 Remote zeroize	1	1A	1AFG	1D	1DF	1DG	1DFG	1G	1F	1FG
3 BLACK SIGNAL CONNECTOR										
3.1 Attention-word	5	-	-	5D	5DF	5DG	5DFG	5G	5F	5FG
3.2 Change crypto var.	6	-	-	6D	6DF	6DG	6DFG	6G	6F	6FG
3.3 Crypto start(ECCM OFF)	-	-	-	-	-	5D	5DF	5	-	5F
3.4 Crypto start(ECCM ON)	5G	-	-	5DG	5DFG	-	-	-	5FG	-
3.5 Compromise	5D	-	-	-	-	-	-	5DG	5DF	5DFG
3.6 Rest	-	-	-	-	-	-	-	-	-	-
4 EFFECT ON OPERATION										
4.1 Transport/sleutel uit	1	1A	1AFG	1	1F	1G	1FG	1G	1F	1FG
4.2 Lamp test	5	-	-	5	5F	5G	5FG	5G	5F	5FG
4.3 Test alarm reset	5A	5FG	5FG	5A	5AF	5AG	5AFG	5AG	5AF	5AFG
4.4 Test toestel	4B	-	-	4B	4BFG	4B	4BFG	4B	4BFG	4BFG
4.5 Base key	4B	-	-	4B	4BF	4BG	4BFG	4BG	4BF	4BFG
4.6 Sleutel laden	5	-	-	5	5F	5G	5FG	5G	5F	5FG
4.7 Change crypto	6E	-	-	6E	6EF	6EG	6EFG	6EG	6EF	6EFG
4.8 Load spare crypto	5	-	-	5	5F	5G	5FG	5G	5F	5FG
4.9 LA Loop	5	-	-	5	5F	5G	5FG	5G	5F	5FG
4.10 Bedrijf (Operation)	-	-	-	5	5F	5G	5FG	-	-	-
4.11 Onderhoud 1	5	-	-	5	5F	5G	5FG	5G	5F	5FG
4.12 Onderhoud 2	4BFG	-	-	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG
4.13 ECCM switch on	5F	-	-	5DF	-	5FG	-	5FG	-	-
4.14 ECCM switch off	-	-	-	-	5D	-	5DG	-	5	5G
5 ALARM	5A	-	-	5AD	5ADF	5ADG	5ADFG	5AG	5AF	5AFG

Table 4-5: Status and changes of status in operational state 5

STATUS (Operational STATE + MODE) / EFFECT OF:	6	6A	6AFG	6B	6BD	6BDF	6BDG	6BDFG	6BF	6BG	6BFG	6D	6DF	6DG	6DFG	6E	6EF	6EG	6EFG	6F	6G	6FG
1 SWITCHING ON	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG	6FG
2 RED SIGNAL CONNECTOR																						
2.1 Sync command	6	-	-	6B	6BD	6BDF	6BDG	6BDFG	6BF	6BG	6BFG	6D	6DF	6DG	6DFG	-	-	-	-	6F	6G	6FG
2.2 Remote zero.	1	1A	1AFG	1	1D	1DF	1DG	1DFG	1F	1G	1FG	1D	1F	1G	1DFG	1	1F	1G	1FG	1F	1G	1FG
3 BLACK SIGNAL CONNECTOR																						
3.1Attent.-word	6	-	-	6	6D	6DF	6DG	6DFG	6F	6G	6FG	6D	6DF	6DG	6DFG	6E	6EF	6EG	6EFG	6F	6G	6FG
3.2Change crypto	6	-	-	*	*	*	*	*	*	*	*	6D	6DF	6DG	6DFG	-	-	-	-	6F	6G	6FG
3.3Crypto start (ECCM off)	6B	-	-	*	*	*	*	*	*	*	*	6DB	6BDF	6BD	6BDF	6B	6BF	6B	6BF	6BF	6B	6BF
3.4Crypto start (ECCM on)	6BG	-	-	*	*	*	*	*	*	*	*	6BDG	6BDFG	6BDG	6BDFG	6BG	6BFG	6BG	6BFG	6BFG	6BG	6BFG
3.5 Compromise	6D	-	-	*	*	*	*	*	*	*	*	6D	6DF	6DG	6DFG	6D	6DF	6DG	6DFG	6DF	6DG	6DFG
3.6 Rest	6B	-	-	-	-	-	-	-	-	-	-	6BD	6BDF	6BDG	6BDFG	-	-	-	-	6BF	6BG	6BFG
4 EFFECT ON OPERATION																						
4.1 Transport/ sleutel uit	1	1A	1AFG	1	1	1F	1G	1FG	1F	1G	1FG	1	1F	1G	1FG	6	6F	6G	6FG	1F	1G	1FG
4.2 Lamp test	6	-	-	6B	6B	6BF	6BG	6BFG	6BF	6BG	6BFG	6	6F	6G	6FG	6	6F	6G	6FG	6F	6G	6FG
4.3 Test alarm reset	6A	6FG	6FG	6A	6A	6AF	6AG	6AFG	6AF	6AG	6AFG	6A	6AF	6AG	6AFG	6	6F	6G	6FG	6AF	6AG	6AFG
4.4 Test toestel	6B	-	-	6B	6B	6BFG	6B	6BFG	6BFG	6B	6BFG	6B	6BFG	6B	6BFG	6	6F	6G	6FG	6BFG	6B	6BFG
4.5 Base key	4B	-	-	4B	4B	4BF	4BG	4BFG	4BF	4BG	4BFG	4B	4BF	4BG	4BFG	6	6F	6G	6FG	4BF	4BG	4BFG
4.6 Sleutel laden	7	-	-	7B	7B	7B	7BG	7BFG	7BF	7BG	7BFG	7	7F	7G	7FG	6	6F	6G	6FG	7F	7G	7FG
4.7 Change crypto	6E	-	-	6E	6E	6E	6EG	6EFG	6EF	6EG	6EFG	6E	6EF	6EG	6EFG	6E	6EF	6EG	6EFG	6EF	6EG	6EFG
4.8 Load spare crypto	7	-	-	7B	7B	7B	7BG	7BFG	7BF	7BG	7BFG	7	7F	7G	7FG	6	6F	6G	6FG	7F	7G	7FG
4.9 LA Loop	6	-	-	6B	6B	6B	6BG	6BFG	6BF	6BG	6BFG	6	6F	6G	6FG	6	6F	6G	6FG	6F	6G	6FG
4.10 Bedrijf (Operation)	-	-	-		6B	6B	6BG	6BFG	-	-	-	6	6F	6G	6FG	6	6F	6G	6FG	-	-	-
4.11 Onderhoud 1	6	-	-	6B	6B	6B	6BG	6BFG	6BF	6BG	6BFG	6	6F	6G	6FG	6	6F	6G	6FG	6F	6G	6FG
4.12 Onderhoud 2	4BFG	-	-	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	-	-	-	-	4BFG	4BFG	4BFG
4.13 ECCM switch on	6F	-	-	6BF	6BDF	-	6BDFG	-	-	6BFG	-	6DF	-	6DFG	-	-	-	-	-	-	6FG	-
4.14 ECCM switch off	-	-	-	-	-	6BD	-	6BDG	6B	-	6BG	-	6D	-	6BG	-	-	-	-	6	-	6G
5 ALARM	6A	-	-	6A	6AD	6ADF	6ADG	6ADFG	6AF	6AG	6AFG	6AD	6ADF	6ADG	6ADFG	6A	6AF	6AG	6AFG	6AF	6AG	6AFG

Table 4-6: Status and changes of status in operational state 6

STATUS (Operational STATE + MODE)	7	7A	7AFG	7B	7BD	7BDF	7BDG	7BDFG	7BF	7BG	7BFG	7C	7CF	7CG	7CFG	7D	7DF	7DG	7DFG	7F	7G	7FG
EFFECT OF:																						
1 SWITCHING ON	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG	7FG
2 RED SIGNAL CONNECTOR																						
2.1 Sync command	7	-	-	7B	7BD	7BDF	7BDG	7BDFG	7BF	7BG	7BFG	7C	7CF	7CG	7CFG	7D	7DF	7DG	7DFG	7F	7G	7FG
2.2 Remote zero.	1	1A	1AFG	1	1D	1DF	1DG	1DFG	1F	1G	1FG	1	1F	1G	1FG	1D	1DF	1DG	1DFG	1F	1G	1FG
3 BLACK SIGNAL CONNECTOR																						
3.1 Attent.-word	7	-	-	7	7D	7DF	7DG	7DFG	7F	7G	7FG	7	7F	7G	7FG	7D	7DF	7DG	7DFG	7F	7G	7FG
3.2 Change crypto	6	-	-	*	*	*	*	*	*	*	*	*	*	*	*	6D	6DF	6DG	6DFG	6F	6G	6FG
3.3 Crypto start (ECCM off)	7B	-	-	*	*	*	*	*	*	*	*	*	*	*	*	7BD	7BDF	7BD	7BDF	7BF	7B	7BF
3.4 Crypto start (ECCM on)	7BG	-	-	*	*	*	*	*	*	*	*	*	*	*	*	7BDG	7BDFG	7BDG	7BDFG	7BFG	7BG	7BFG
3.5 Compromise	7D	-	-	*	*	*	*	*	*	*	*	*	*	*	*	7D	7DF	7DG	7DFG	7DF	7DG	7DFG
3.6 Rest	7B	-	-	*	*	*	*	*	*	*	*	*	*	*	*	7BD	7BDF	7BDG	7BDFG	7BF	7BG	7BFG
4 EFFECT ON OPERATION																						
4.1 Transport/ sleutel uit	1	1A	1AFG	1	1	1F	1G	1FG	1F	1G	1FG	7B	7BF	7BG	7BFG	1	1F	1G	1FG	1F	1G	1FG
4.2 Lamp test	7	-	-	7B	7B	7BF	7BG	7BFG	7BF	7BG	7BFG	7B	7BF	7BG	7BFG	7	7F	7G	7FG	7F	7G	7FG
4.3 Test alarm reset	7A	7FG	7FG	7A	7A	7AF	7AG	7AFG	7AF	7AG	7AFG	7B	7BF	7BG	7BFG	7A	7AF	7AG	7AFG	7AF	7AG	7AFG
4.4 Test toestel	7B	-	-	7B	7B	7BFG	7B	7BFG	7BFG	7B	7BFG	7B	7BF	7BG	7BFG	7B	7BFG	7B	7BFG	7BFG	7B	7BFG
4.5 Base key	4B	-	-	4B	4B	4BF	4BG	4BFG	4BF	4BG	4BFG	7B	7BF	7BG	7BFG	4B	4BF	4BG	4BFG	4BF	4BG	4BFG
4.6 Sleutel laden	7	-	-	7B	7B	7BF	7BG	7BFG	7BF	7BG	7BFG	7B	7BF	7BG	7BFG	7	7F	7G	7FG	7F	7G	7FG
4.7 Change crypto	6E	-	-	6E	6E	6EF	6EG	6EFG	6EF	6EG	6EFG	7B	7BF	7BG	7BFG	6E	6EF	6EG	6EFG	6EF	6EG	6EFG
4.8 Load spare crypto	7	-	-	7B	7B	7BF	7BG	7BFG	7BF	7BG	7BFG	7B	7BF	7BG	7BFG	7	7F	7G	7FG	7F	7G	7FG
4.9 LA Loop	7	-	-	7B	7B	7BF	7BG	7BFG	7BF	7BG	7BFG	7B	7BF	7BG	7BFG	7	7F	7G	7FG	7F	7G	7FG
4.10 Bedrijf (Operation)	-	-	-	7C	7C	7CF	7CG	7CFG	7CF	7CG	7CFG	7C	7CF	7CG	7CFG	7	7F	7G	7FG	-	-	-
4.11 Onderhoud 1	7	-	-	7B	7B	7BF	7BG	7BFG	7BF	7BG	7BFG	7B	7BF	7BG	7BFG	7	7F	7G	7FG	7F	7G	7FG
4.12 Onderhoud 2	4BFG	-	-	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	7B	7BF	7BG	7BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG	4BFG
4.13 ECCM switch on	7F	-	-	7BF	7BDF	-	7BDFG	-	-	7BFG	-	7CF	-	7CFG	-	7DF	-	7DFG	-	-	7FG	-
4.14 ECCM switch off	-	-	-	-	-	7BD		7BDG	7B	-	7BG	-	7C	-	7CG	-	7D	-	7DG	7	-	7G
5 ALARM	7A	-	-	7A	7AD	7ADF	7ADG	7ADFG	7AF	7AG	7AFG	7A	7AF	7AG	7AFG	7AD	7ADF	7ADG	7ADFG	7AF	7AG	7AFG

Table 4-7: Status and changes of status in operational state 7

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

DISPLAY INDICATIONS

Survey of indications as displayed depending upon the crypto variable settings, the rotary function selector and the button ACTIVATE.

Equipment modes:
1 No crypto variables present
2 Transmit compromise
3 Base key in operational crypto variable register
4 Base key as operational crypto variable and a spare crypto variable present
5 A crypto variable present as a spare crypto variable
6 The same crypto variable as an operational and as spare crypto variable present
7 Aspare and an operational crypto variable present
8 Compromise received
9 Alarm

Rotary function selector	Equipment state								
	1	2	3	4	5	6	7	8	9
TRANSPORT	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	COMP	AL
Activate pressed	blank	ZERO ::::	blank	blank	blank	blank	blank	ZERO	ZERO
Later	ZERO ::::	ZERO ::::	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	AL
LAMP	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	COMP	AL
during Activate	**** 0000 ::::	ZERO ::::	**** 0000 ::::	**** 0000 ::::	**** 0000 ::::	**** 0000 ::::	**** 0000 ::::	**** 0000 ::::	AL
Later	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	1)	AL
Alarm reset	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	COMP	AL
After Activate pressed	AL blank	ZERO ::::	AL blank	AL blank	AL blank	AL blank	AL blank	AL	Origin. info

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

Rotary function selector	Equipment mode 1	2	3	4	5	6	7	8	9
TOESTEL	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	COMP	AL
Activate pressed	TEST	ZERO ::::	TEST	TEST	TEST	TEST	TEST	TEST	AL
If test correct	OK TEST	n/a	OK TEST	OK TEST	OK TEST	OK TEST	OK TEST	n/a	n/a
If error	****	n/a	****	****	****	****	****	n/a	n/a
BASE	ZERO	ZERO ::::	B SL	SL+B .	SL L	SL W	R+SL	COMP	AL
Activate pressed	blank	ZERO ::::	blank	blank	blank	blank	blank	2)	AL
Later	B SL	ZERO ::::	B SL	SL+B	SL+B	SL+B	SL+B	1)	AL
LOAD	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	COMP	AL
Activate pressed	blank	ZERO ::::	blank	blank	blank	blank	blank	2)	AL
Later	SL L	ZERO ::::	SL+B	SL+B	SL L	R+SL	R+SL	1)	AL
CHANGE	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	COMP	AL
Activate pressed	ZERO	ZERO ::::	ZERO	blank	blank	blank	blank	2)	AL
Later	ZERO	ZERO ::::	B SL	SL W ::::	SL W ::::	SL W ::::	SL W ::::	2)	AL
Correct	n/a	n/a	n/a	SL W	SL W	SL W	SL W	1)	AL
RES LOAD	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	COMP	AL
Activate pressed	blank	ZERO ::::	blank	blank	blank	blank	blank	2)	AL
Later	SL L	ZERO ::::	SL+B	SL+B	SL L	R+SL	R+SL	1)	AL

Rotary function selector	Equipment mode 1	2	3	4	5	6	7	8	9
LA	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	COMP	AL
After activate pressed	LUS	ZERO	LUS	LUS	LUS	LUS	LUS	LUS	AL
BEDRIJF	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	blank	COMP	AL
After activate pressed	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	blank	1)	AL
ONDERHOUD 1	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	COMP	AL
Activate pressed	blank	ZERO ::::	blank	blank	blank	blank	blank	2)	AL
Later	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	1)	AL
ONDERHOUD 2	ZERO	ZERO ::::	B SL	SL+B	SL L	SL W	R+SL	COMP	AL
Activate pressed	code	ZERO ::::	code	code	code	code	code	code	AL
If test correct	OK	n/a	OK	OK	OK	OK	OK	OK	n/a
If error	code	n/a	code	code	code	code	code	code	n/a

1) Indication depends on status.

2) Indication depends on present crypto variables.

DATA BYTES.

ALMDEL	Register to delay the de-energise of alarm relay
BLKDEL1	Contains display value: blank, crypto variable setting or COMP
BLKDEL2	Counter. If zero, then BLKDEL1 is decreased with 1
CNSTTE	Counts number of equal nibbles
CTRTBA	Begin address tabel with diagnostic information
DGNINP	Diagnostic input used during diagnostic test
DSPOFS	Offset of the last displayed indication
DSPTBA	Begin address display tabel
ISBGAD	Begin address spare crypto variable memory
ISBUAD	Begin address spare crypto variable buffer
ISTBY1A	Internal status byte 1A
ISTBY1B	Internal status byte 1B
ISTBY2	Internal status byte 2
ISTBY3	Internal status byte 3
ISTBY4	Internal status byte 4
LTCYTE	Cycles counter in module LMPTST
LTDLTE	Delay counter in module LMPTST
RDADRS	Address random memory
RDBGAD	Begin address random memory
RDBITE	Random bit counter
RDENAD	End address random memory
RDLAST	Last read crypto bit for random memory
RNDCHC	Check byte random memory
STCHNB	Check byte valid base key
STFRBE	Last selected data from front control
STPAEH	Last send data to POPAEH
STSTBI	Last send data to POSTBI
STSTLD	Last valid data send to POSTLD
STTEDA	Last data send to POTEDA
SYNCCO	Last read information sync category
SYNCOU	Counter to check if adjusted reaction time is passed
SYREDE	Buffer with repetition delay time
SYREDR	Adjusted reaction time sync category 3
SYRETW	Adjusted reaction time sync category 2
SYRPDE	Buffer with repetition delay time
SYRPDR	Adjusted repetition time sync category 3
SYRPTW	Adjusted repetition time sync category 2
WGBGAD	Begin address operational crypto variable memory

Layout internal status bytes.

ISTBY1A	D0	ISWS	Set if operational and spare crypto variable equal
	D1	WSAF	Set if no operational crypto variable
	D2	ISAF	Set if no spare crypto variable
	D3	BSSL	Set if operational crypto variable register contains base key
ISTBY1B	D0	NOVE	Set in module NORVER
	D1	TELU	Set if test loop is switched on
	D2	INSY	Set if receiver is synchronous
	D3	ACTV	Set if button ACTIVATE is pressed
ISTBY2	D0	ECMZ	Set if ECCM switch is on
	D1	ECMR	Set if contrary post has ECCM switch on
	D2	COZE	Set if in compromise transmit mode
	D3	ALTE	Set if in alarm mode
	D4	ACTT	Set if button Activate is pressed
	D5	SWPA	Set if change crypto variable pattern recognised
	D6	COPA	Set if compromise pattern recognised
	D7	CSPA	Set if crypto start pattern recognises
ISTBY3	D0	SLFO	Set if crypto variable not valid
	D1	IRZF	Set if error in register transmitter key generator
	D2	IROF	Set if error in register receiver key generator
	D3	SWGF	Set if error in crypto variable memory after change crypto variable
	D4	SWZF	Set if error in transmitter key generator after change crypto variable
	D5	SWOF	Set if error in receiver key generator after change crypto variable
	D6	TEFO	Set if error detected during test
	D7	TEMO	Set if in test mode
ISTBY4	D0	SLWP	Set if transmitter in change crypto variable procedure
	D1	RNDM	Random memory

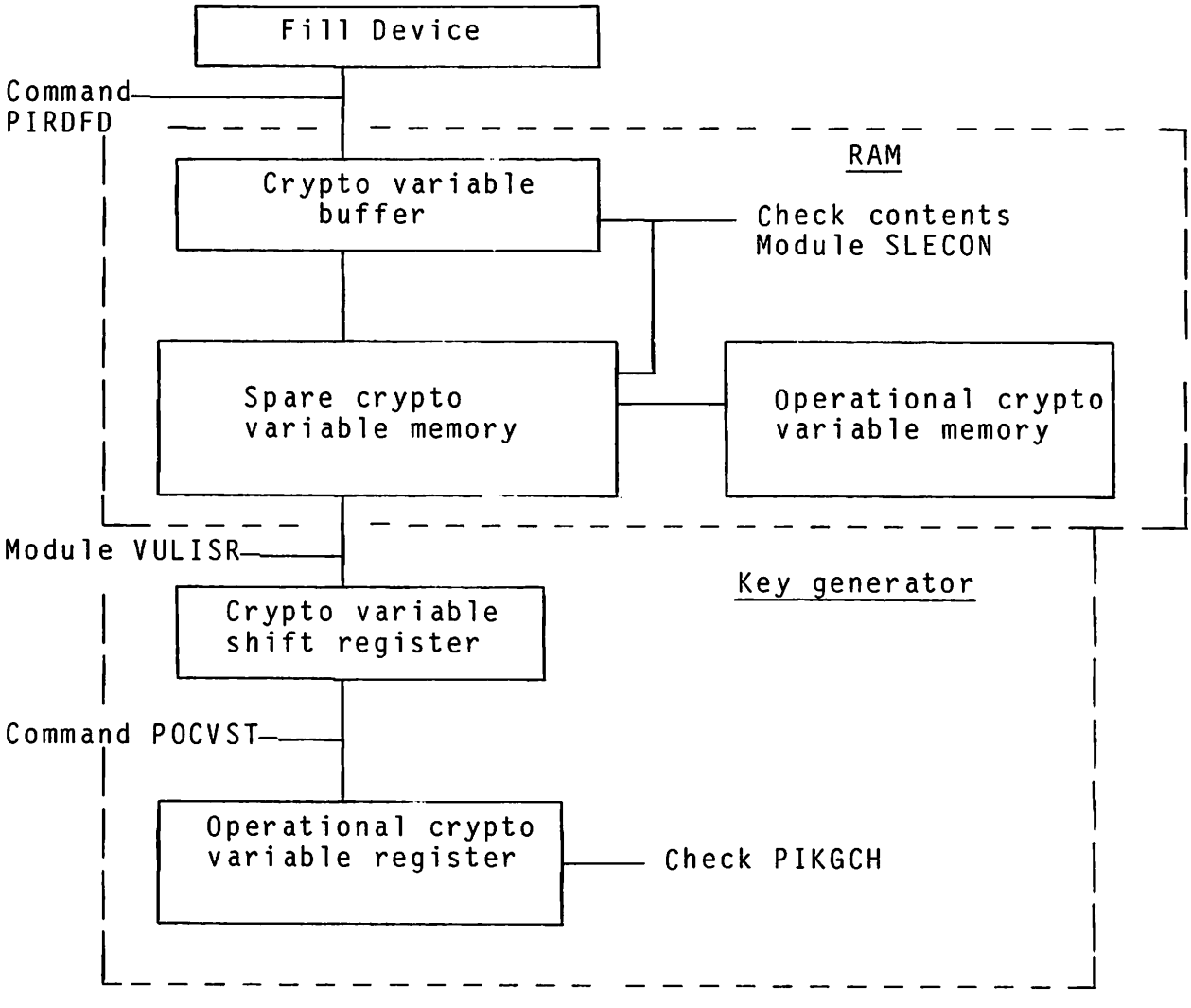
NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

Function INPUT GATES

PIKGCH	Key generator check
PIPEST	Pattern unit status
PIRDFD	Read fill device
PIFRBE	Front controls
PIADBY	Adjust byte
PISYCO	Synchronisation command
PIDAOB	Data out bus

Function OUTPUT GATES

POCVCP	Crypto variable clock pulse
POCVST	Crypto variable strobe
POPAEH	Pattern unit
POTEDA	Test data
POSTLD	Status and leds
PODISP	Display
POSTBI	Set black interface



NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
INITIA    BEGIN (INITIA)
100       Block red interface (POTEDA)
          Reset pattern recognition circuit (POPAEH)
          Block alarm circuit (POPAEH)
          Energise alarm relay and loop relay (POSTBI)
          Reset RST 7.5
          Force POSTLD
                All leds lit
                External status: synchronous=0
                                 Normal traffic=0
                                 Secured connection=0
          Display TEST (PODISP)
          Test stackpointer
          IF error
            THEN
              Stop program
          ENDIF
105       Set stackpointer
          Test CPU, ROM, RAM and internal data bus (Module CPUTST)
          Delaytime for reading display indication
          Define offset display (DSPOFS)
          Define internal status (ISTBY1B, ISTBY2, ISTBY3, ISTBY4)
          ISTBY1B: ACTV=0, INSY=0, TELU=0, NOVE=0
          ISTBY2:  CSPA=0, COPA=0, SWPA=0, ACTT=1,
                   ALTE=0, COZE=0, ECMR=1, ECMZ=1,
          ISTBY3:  TEMO=0, TEFO=0, SWOF=0, SWZF=0
                   SWGF=0, IROF=0, IRZF=0, SLFO=0,
          ISTBY4:  SLWP=0, RNDM=0
          Define databytes (STSTLD, STPAEH, STTEDA)
          STSTLD: Fill device not selected
                  Led SYNC ALARM lit
                  Led ECCM lit
                  Led BEDRIJF extinguished
                  External status =0
          STTEDA: Red data not controlled by µ processor
                  Block red data output
                  Data clock controlled by µ processor
                  No loop at red interface
          Send STTEDA (POTEDA)
          STSTBI: Loop relay energised, alarm relay de-energised
          STPAEH: Message key register connected as a rotary shift
                                          register
                  Reset alarm circuit
                  Reset pattern recognition circuit
                  No test loop at black interface
                  Pattern recognition in code rest
                  ECCM switched on
          Pattern generator in rest mode
          Test stackpointer and M-registers
          Test message key registers and alarm circuitry (Module
                                              BRATST)
          IF fault (TEFO=1)
            THEN
105.1         Set ACCT=0
              Read front controls (Module REFRBE)
```

```
            IF ACTV=0
             THEN
105.1.1        Go to 105.1
             ENDIF
          ENDIF
110       Set ACTV=0, Initiate transmit key generator.
          Set STTEDA
              Data clock controlled by data clock control
          Send STTEDA (POTEDA)
          Set pattern generator in rest mode
          Block crypto and alarm circuitry (POPAEH)
          Reset RST 7.5
          De-energise alarm relay (POSTBI)
          Display BUSY
          Wait ca 4 seconds for synchronisation
          Loop relay de-energised (POSTBI)
          Release red interface and block red data
120       IF check nibbles OK
           THEN
120.1         BSSL=1
              Set internal status WSAF=1 and ISWS=0
              Read crypto variable shift registers with base key
                                              (Module VULISR)
              IF crypto variable shift registers correct (IROF=0,
                                                  IRZF=0)
               THEN
120.1.1           Read operational crypto variable registers with
                  contents crypto variable shift registers (POCVST)
                  Read key generators (PIKGCH)
                  IF reading correct at transmitter and receiver part
                   THEN
                      Go to 130
                  ENDIF
              ENDIF
120.2         Set internal status BSSL=0
          ENDIF
130       IF internal status ISAF=0
           THEN
              IF contents valid (SLFO=0)
               THEN
130.1           Test validity crypto variable memory (Module SLECON)
130.1.1         IF internal status WSAF=0
                 THEN
                    Set internal status BSSL=0
                    Test validity operational crypto variable (Module
                                                        SLECON)
                    IF contents valid (SLFO=0)
                     THEN
                        Read crypto variable shift register with spare
                        crypto variable memory key memory
                        IF crypto variable shift register correct
                                                  (IROF=0,IRZF=0)
                         THEN
                            Read contents in operational crypto
                                          variable register
                            Read key generators (PIKGCH)
                            IF reading correct at transmitter and
                                       receiver part
```

```
                                THEN
                                  Go to 130.1.2
                              ENDIF
                           ENDIF
                        ENDIF
                        Set internal status WSAF=1 and ISWS=0
                        Zeroïze contents operational crypto variable
                                                        memory
                    ENDIF
130.1.2             Read crypto variable shift registers with contents
                          spare crypto variable memory (Module VULISR)
                    IF reading correct (IROF=0 and IRZF=0)
                      THEN
                        Go to 150
                    ENDIF
                  ENDIF
              ENDIF
140           Set internal status ISAF=1, WSAF=1, ISWS=0
              Zeroïze operational and spare crypto variable memory
150           IF internal status ISWS=1
                THEN
150.1             IF valid crypto variables (WSAF=0, ISAF=0)
                    THEN
150.1.1               Compare contents operational crypto variable
                          register with crypto variable shift registers
                      IF contents equal
                        THEN
                          Go to 160
                      ENDIF
                  ENDIF
150.2             Set internal status ISWS=0
              ENDIF
155           Display crypto variable settings (Module DSPSLI)
              IF base key present
                THEN
                  Go to 160.2
              ENDIF
160           IF spare and operational crypto variable present
                THEN
160.1             Set databyte STSTLD:
                                External status: Secured connection
160.2             Set databyte STTEDA:
                                Release red data output
                  Send STTEDA (POTEDA)
                  Set databyte STSTLD:
                              External status: synchronous =1
                              Extinguish led SYNC ALARM
                  Set internal status INSY=1
                  Release crypto output and alarm circuit (POPAEH)
              ENDIF
170           Send leds indication and external status (POSTLD)
              Read and calculate synchronisation times
                        SYRETW=0
                        SYRPTW = Trep 1
                        SYREDR = Treac
                        SYRPDR = Trep 2 (Module SYNCT)
              Reset counters (SYNCOU, SYREDE, SYRPDE)
```

```
          Set databytes:
                          BLKDEL1=00
                          BLKDEL2=00
                          RDBITE =00
                          LTCYTE =00
                          LTDLTE =50
                          SYNCCO = category 1
          Set RDADRS = RDBGAD
          Read ECCM switch
          IF ECCM switch in position off
            THEN
170.1         Set ECMZ=0
          ENDIF
180       Read databyte STPAEH
          Release pattern recognition (POPAEH)
          Release Attention-word and alarm interrupt
          Go to module MAINMO
          END (INITIA)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
MAINMO    BEGIN (MAINMO)
1000      Read front controls (Module REFRBE)
          IF button ACTIVATE has been pressed (ACTV=1)
            THEN
              Set internal status COPA=0
              Read random bits into random  memory (Module RFRRND)
          ENDIF
1010      IF in mode transmit compromise (COZE=1)
            THEN
1010.1        IF compromise is recognised 2 times (COPA=1)and activate
                                  not pressed
                THEN
                  Display COMP
              ENDIF
              IF compromise is not recognised 2 times (COPA=0)
                THEN
                  Display ZERO (Module DSPLAY)
                  Time delay 1 second
                  Display :::: (Module DSPLAY)
                  Time delay 1 second
                  Reset status activate
              ENDIF
1010.2    Go to 1000
          ENDIF
1100      Go to module SYNCPR
2000      Go to module FROBED
2200      IF remote zeroïze active
            THEN
2200.1        Go to module REMZER
              Release interrupts
              Wipe display during ca 0.1 second
              Display ZERO during ca 0.5 second
          ENDIF
2220      IF no base key or crypto variable present
            THEN
              IF not in compromise transmit mode
                THEN
                  Set STSTLD External status: not secure connection
                                              not synchronous
                                              not normal traffic
                  Led: SYNC ALARM lit
                       Normal traffic extinguished
              Block crypto output
              Block red data receiver output
              ENDIF
          ENDIF
2230      Go to 1000
          END (MAINMO)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
SYNCPR    BEGIN (SYNCPR)
1110      Read sync category (PISYCO)
          IF sync category 3
            THEN
              Mask SNB
              Set databyte STSTLD
                           Led SYNC ALARM lit
              Compare new command with previous command (SYNCCO)
              IF a new sync category
                THEN
                  Reset SYNCOU
                  Force SYREDE equal to SYREDR
                  Force SYRPDE equal to SYRPDR
              ENDIF
              Go to 1140
          ENDIF
1120      IF in sync mode (INSY=1)
            THEN
              Set databyte STSTLD
                           Led SYNC ALARM extinguished
          ENDIF
1130      IF sync category 2
            THEN
              Compare new command with previous command (SYNCCO)
              IF a new category
                THEN
                  Reset SYNCOU
                  Force SYREDE equal to SYRETW
                  Force SYRPDE equal to SYRPTW
              ENDIF
          ENDIF
1140      IF sync category is not category 1
            THEN
              Increase SYNCOU
              IF SYNCOU is not less than SYREDE
                THEN
                  Reset SYNCOU
                  Force SYREDE = SYRPDE
              ENDIF
              IF operational crypto variable or base key present
                THEN
                  Transmit crypto start pattern (Module ZECRST)
              ENDIF
              Time delay 1 msecond (Module DELAY)
              Go to 1160
          ENDIF
1150      Renew contents Random memory
1160      Store read command in SYNCCO
1170      Release Attention-word interrupt
          Go to 2000 (Module FROBED)
          END (SYNCPR)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
FROBED    BEGIN (FROBED)
2000      IF ECCM switch in position on
            THEN
              IF ECCM switch was switched off (ECMZ=0)
                THEN
                  Set internal status ECMZ=1
                  Transmit crypto start pattern (ZECRST)
              ENDIF
          ENDIF
2002      IF ECCM switch in position off
            THEN
              IF ECCM switch was in position on
                THEN
                  Set internal status ECMZ=0
                  Transmit crypto start pattern (ZECRST)
              ENDIF
          ENDIF
2004      Set databyte STSTLD
                       Extinguish led ECCM
          IF ECCM switch and ECCM switch contrary post in position on
           THEN
             Set data byte STSTLD
                           led ECCM lit
          ENDIF
2008      IF rotary function selector not in position BEDRIJF
            THEN
              Set data byte STSTLD
                            Set external status: Normal traffic=0
                            Extinguish led BEDRIJF
              Energise alarm relay
          ENDIF
2010      IF rotary function selector in position LAMP
            THEN
              IF button ACTIVATE pressed
                THEN
                  Go to 2020
              ENDIF
          ENDIF
2015      Send indication leds and external status (POSTLD)
          Reset LTCYTE
          Load LTDLTE
2020      IF testloop switched on (TELU=1)
            THEN
              IF rotary function selector not in position LA
                THEN
                  Disconnect clock and data in- and output at the
                                        encryption part (POSTBI)
                  Set internal status TELU=0
              ENDIF
          ENDIF
2030      IF action was finished within ca 1 second (BLKDEL1 not 0)
            THEN
              Force ACTV = 0
              Decrease BLKDEL2 with 1
              IF BLKDEL2 = 0
                THEN
                  Decrease BLKDEL1 with 1
```

```
                Force BLKDEL2 = 8
            ENDIF
            Go to 2170
        ENDIF
2050    IF rotary function selector in position BEDRIJF
          THEN
            Go to module NORVER
        ENDIF
2060    IF rotary function selector in position SLEUTEL WISSEL
          THEN
            Go to module SLWBED
        ENDIF
2070    IF rotary function selector in position SLEUTEL LADEN
          THEN
            Go to module SLLADE
        ENDIF
2080    IF rotary function selector in position TRANSPORT
          THEN
            Go to module SLUIT
        ENDIF
2090    IF rotary function selector in position LAMP
          THEN
            Go to module LMPTST
        ENDIF
2100    IF rotary function selector in position ONDERHOUD 1
          THEN
           Go to module START
2110    IF rotary function selector in position SLEUTEL BASIS
          THEN
            Go to module BASSLE
        ENDIF
2120    IF rotary function selector in position SLEUTEL RES LADEN
          THEN
            Go to module SLLADE
        ENDIF
2130    IF rotary function selector in position LA
          THEN
            Go to module TSTLUS
        ENDIF
2140    IF rotary function selector in position ONDERHOUD 2
          THEN
            Go to module DGNTST 1, 2, 3, 4
        ENDIF
2150    IF rotary function selector in position ALARM RESET
          THEN
            Go to module ALMTST
        ENDIF
2160    IF rotary function selector in position TOESTEL
          THEN
            Go to module FNCTST
        ENDIF
2170    Set internal status ACTV=0
        Go to 2200 (Module MAINMO)
        END (FROBED)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
NORVER    BEGIN (NORVER)
2050.1    Set internal status NOVE=1
          Display crypto variable settings (Module DSPSLI)
          IF spare and operational crypto variable present (WSAF=0,
                                    ISAF=0) and unequal (ISWS=0)
            THEN
              IF synchronous (INSY=1)
                THEN
                  Set databyte STSTLD
                               led BEDRIJF lit
                               external status: Normal traffic
                  Send STSTLD(POSTLD)
                  IF ALMDEL not 0
                    THEN
                      Decrease ALMDEL
                      Go to 2050.2
                  ENDIF
               ENDIF
          ENDIF
2050.2    Go to 2170 (Module FROBED)
          END (NORVER
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
SLWBED    BEGIN (SLWBED)
2060.10   IF button ACTIVATE pressed (ACTV=1)
            THEN
2060.10.1     IF spare crypto variable present (ISAF=0)
                THEN
2060.10.1.1       Mask Attention-word interrupt
                  Display Blank (Module DSPLAY)
                  Wipe display during ca 1 second (Module BLKDEL)
                  Set databyte STSTLD
                               led SYNC ALARM lit
                               External status: synchronous =0
                                                Secured connection =0
                  Read POSTLD with STSTLD
                  Set databyte STTEDA
                               Block data receiving part
                  Read POTEDA with STTEDA
                  Set internal status CSPA=0, INSY=0, SLWP=1
                  Change crypto variable (Module SLEWSL)
                  IF changing correct (SWGF=0, SWOF=0, SWZF=0)
                    THEN
2060.10.1.1.1         Set databyte STSTLD
                                   External status: Secured connection=1
                      Send POSTLD
                      Release crypto output (POPAEH)
2060.10.1.1.2         Transmit crypto variable change pattern (POPAEH)
                      Start delay of 20 mseconds
                      Release Attention-word interrupt
                  ENDIF
2060.10.1.1.3     IF crypto start pattern not received (CSPA=1)
                    THEN
2060.10.1.1.3.1       IF 20 mseconds not yet passed
                        THEN
                          Go to 2060.10.1.1.3
                      ENDIF
2060.10.1.1.3.2       IF compromise recognised (COPA=1)
                        THEN
                          Go to 2060.10.2
                      ENDIF
2060.10.1.1.3.3       Decrease BLKDEL1
                      IF BLKDEL1=0
                        THEN
                          IF display COMP
                            THEN
                              Go to 2060.10.1.1.3.4
                          ENDIF
                          IF display SL W
                            THEN
                              Display :::: (Module DSPLAY)
                              Load BLKDEL1
                              Go to 2060.10.1.1.3.4
                          ENDIF
                          Display SL W (Module DSPLAY)
                          Load BLKDEL1
                      ENDIF
```

```
2060.10.1.1.3.4       Read front controls (Module REFRBE)
                      IF rotary function selector in position SLEUTEL
                                          WISSEL (Change crypto variable)
                        THEN
                          Go to 2060.10.1.1.2
                      ENDIF
                   ENDIF
                   Set databyte STTEDA
                                Release red data output
                   Read POTEDA with STTEDA
                   Set databyte STSTLD
                                 External status: synchronous=1
                                 Led SYNC ALARM extinguished
                   Send STSTLD
                   Set internal status INSY=1
                ENDIF
2060.10.2       Set BLKDEL1 (Module BLKDSP)
                Go to 2060.30
             ENDIF
2060.20      Release Attention-word interrupt
             Display crypto variable settings (Module DSPSLI)
2060.30      Set internal status SLWP=0
             Go to 2170 (Module FROBED)
             END (SLWBED)
```

```
SLLADE     BEGIN (SLLADE)
2070.1     IF button ACTIVATE pressed down
             THEN
2070.1.1       Read fill device (PIRDFD)
               IF fill device present
                THEN
2070.1.1.10       Mask Attention-word interrupt
                  Display Blank (Module DSPLAY)
                  Preset start address crypto variable buffer (ISBUAD)
                  Force BYTE=32
                  Force BITE=4
                  Reset key byte register (SLBR)
                  Data request pulse to fill device (POSTLD)
               ENDIF
2070.1.1.20    Load period counter register 740 /usec
2070.1.1.30    Read fill device (PIRDFD)
               IF fill-clock low (key bit instable)
                 THEN
                   Decrease PETE
                   IF PETE is not 0
                     THEN
                       Go to 2070.1.1.30
                   ENDIF
                   Request to fill device inactive
                   Go to 2070.1.1.100
               ENDIF
2070.1.1.40    Store bit in SLBR
               Shift SLBR 1 time
               Decrease BITE
               IF BITE=0
                 THEN
                   Store SLBR in crypto variable buffer
                   Increase buffer address
                   Force BITE=4
                   Decrease BYTE
                   IF BYTE=0
                     THEN
                       Request to fill device inactive
                       Go to 2070.1.1.80
                   ENDIF
               ENDIF
2070.1.1.50    Load period counter register 740 /useconds (PETE)
2070.1.1.60    Read fill device (PIRDFD)
               IF fill-clock high (key bit still stable)
                 THEN
                   Decrease PETE
                   IF PETE is not 0
                     THEN
                       Go to 2070.1.1.60
                   ENDIF
                   Request to fill device inactive
                   Go to 2070.1.1.100
               ENDIF
2070.1.1.70    Go to 2070.1.1.20
```

```
2070.1.1.80   Check contents crypto variable buffer (Module SLECON)
              IF contents is valid (SLF0=0)
                THEN
                  Set internal status ISAF=1, ISWS=0
                  Store contents crypto variable buffer in spare
                                              crypto variable memory
                  Check spare crypto variable memory
                  IF spare crypto variable memory correct
                    THEN
                      Store new crypto variable in crypto variable
                                             shift register (Module VULISR)
                      IF no error (IR0F=0, IRZF=0)
                        THEN
                          Set internal status ISAF=0
                          Wipe display during 1 second (Module BLKDSP)
                      ENDIF
                  ENDIF
              ENDIF
2070.1.1.100  Release Attention-word interrupt
              Go to 2070.30
          ENDIF
2070.20   Display crypto variable settings (Module DSPSLI)
2070.30   Go to 2170 (Module FROBED)
          END (SLLADE)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
SLUIT      BEGIN (SLUIT)
2080.10    IF button ACTIVATE is pressed (ACTV=1)
                THEN
2080.10.1         Display Blank (Module DSPLAY)
                  IF no spare crypto variable (ISAF=1) and no base key
                                                      (BSSL=0)
                    THEN
                      Read databyte STPAEH
                      Set internal status COZE=1
                      Release crypto output (POPAEH)
                      Transmit continuous compromise pattern
                                  (Module ZNDPTR)
                      Go to 2080.10.3
                  ENDIF
2080.10.2         Zeroïze the crypto variables (Module REMZER)
2080.10.3         Wipe display during ca 1 second (Module BLKDEL)
                  Go to 2080.30
           ENDIF
2080.20    Display crypto variable settings (Module DSPSLI)
2080.30    Go to 2170 (Module FROBED)
           END (SLUIT)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
LMPTST     BEGIN (LMPTST)
2090.10    IF button ACTIVATE pressed (ACTT=1)
             THEN
2029.10.1      All leds lit(POSTLD)
               IF LTCYTE less than 8
                 THEN
                   Offset display **** (Module DSPLAY)
                   Go to 2090.10.4
               ENDIF
2090.10.2      IF LTCYTE less than 16
                 THEN
                   Offset display 0000 (Module DSPLAY)
                   Go to 2090.10.4
               ENDIF
2090.10.3      Offset display :::: (Module DSPLAY)
2090.10.4      Display offset
               Decrease LTDLTE
               IF LTDLTE=0
                 THEN
                   Load LTDLTE
                   IF SYNC command not category 1
                     THEN
                       Add contents LTDLTE to LTDLTE
                   ENDIF
                   Increase LTCYTE
                   IF LTCYTE is more than 24
                     THEN
                       Reset LTCYTE
                   ENDIF
               ENDIF
2090.10.5      Go to 2090.30
           ENDIF
2090.20    Display crypto variable settings (Module DSPSLI)
           Send STSTLD (POSTLD)
2090.30    Go to 2170 (Module FROBED)
           END (LMPTST)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
START     BEGIN (START)
2100.10   IF button ACTIVATE is pressed (ACTV=1)
            THEN
2100.10.1     Release crypto output (POPAEH)
              Transmit crypto start pattern (Module ZECRST)
              Load counter
2100.10.2     IF pattern has been transmitted
                THEN
                  Display Blank (Module DSPLAY)
                  Set BLKDEL (Module BLKDSP)
                  Go to 2100.10.3
              ENDIF
              Decrease counter
              IF counter not 0
                THEN
                  Go to 2100.10.2
              ENDIF
2100.10.3     IF operational crypto variable and base key absent
                THEN
                  Block crypto output (POPAEH)
              ENDIF
2100.10.4     Go to 2100.30
          ENDIF
2100.20   Display crypto variable settings (Module DSPSLI)
2100.30   Go to 2170 (Module FROBED)
          END (START)
```

```
BASSLE    BEGIN (BASSLE)
2110.10   IF button ACTIVATE has been pressed (ACTV=1)
            THEN
2110.10.1     Display Blank (Module DSPLAY)
              Mask Attention-word interrupt
              Read base key in crypto variable shift register
                                                  (Module VULISR)
              IF reading error (IROF=1 or IRZF=1)
                THEN
                  Go to 2110.10.3
              ENDIF
2110.10.2     Set STSTLD
                  led SYNC ALARM lit
                  External status: Secured connection=0
                                   synchronous=0
              Set internal status: WSAF=1, ISWS=0, INSY=0
              Load operational crypto variable registers with
                contents crypto variable shift register (POCVST)
              Read key generators (PIKGCH)
              IF no reading errors
                THEN
                  Set STSTLD
                      External status: Secured connecton=0
                                       synchronous=1
                  Set internal status BSSL=1, INSY=1
                  Set check nibbles
                  Release red data output (POTEDA)
                  Release crypto output and alarm circuit(POPAEH)
                  IF sync command not in category 3
                    THEN
                      Set databyte STSTLD
                                   Led SYNC ALARM extinguished
                  ENDIF
              ENDIF
2110.10.3     Read POSTLD with STSTLD
               IF spare crypto variable present (ISAF=0)
               THEN
                  Set internal status ISAF=1
                  Read crypto variable shift register with spare
                                    crypto variable (Module VULISR)
                    IF Reading correct(IROF=0,IRZF=0)
                      THEN
                        Set internal status ISAF=0
                    ENDIF
               ENDIF
2110.10.4      Set BLKDEL (Module BLKDSP)
               Release Attention-word interrupt
               Go to 2110.30
          ENDIF
2110.20   Display crypto variable settings (Module DSPSLI)
2110.30   Go to 2170 (Module FROBED)
          END (BASSLE)
```

```
TSTLUS    BEGIN (TSTLUS)
2130.10   IF testloop not switched on (TELU=0)
            THEN
              IF button ACTIVATE pressed   (ACTV=1)
                THEN
                  Display Blank (Module DSPLAY)
                  Set internal status TELU=1
                  Connect data and clock inputs and outputs
                            (energise crypto loop relay) (POSTBI)
          Set BLKDEL (Module BLKDSP)
                  Go to 2130.30
              ENDIF
              Display crypto variable settings (Module DSPSLI)
              Go to 2130.30
          ENDIF
2130.20   Display LUS
2130.30   Go to 2170 (Module FROBED)
          END (TSTLUS)
```

```
DGNTST1   BEGIN (DGNTST1)
2140.10   IF button ACTIVATE has been pressed
            THEN
2140.10.10    Mask Attention-word interrupt
              Set databyte STSTLD
                          External status: Sync alarm =1
                                           Normal operation =0
                                           Secured connection =0
                                           All leds lit
              Send STSTLD
              Connect output to input black signals (POSTBI)
              Set databyte STTEDA
                   Data clock controlled by /u processor
                   Connect data output to input red signals
                   Connect red transmitter to receiver clock
                   Connect sync command line with red data input
                   Data input ECCM circuit controlled by /u p
                   Connect sync command line to red data
                   Release red data
              Send STTEDA (POTEDA)
              Read time adjustments (straps) (PIADBY)
              Create display message due to strap settings
              Display strap settings
              Wait ca 3 seconds (Module DELAY)
2140.10.20    Display during 2 seconds **** (Modules DSPLAY/DELAY)
              Display during 2 seconds 0000 (Modules DSPLAY/DELAY)
              Display during 2 seconds :::: (Modules DSPLAY/DELAY)
              Display 2 01 (Module DSPLAY)
              Test CPU, RAM, ROM, internal data bus (Module CPUTST)
2140.10.30    Display 4 02 (Module DSPLAY)
              Set internal status ECMR=1, ECMZ=1, TEFO=1, TEMO=1
              Test message key register and alarm circuit (Module
                                                   BRATST)
              IF fault (TEFO=1)
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.40    Display 3 03 (Module DSPLAY)
              Read in crypto variable shift register the base key
                                              (Module VULISR)
              IF shift in transmitter part incorrect (IRZF=1)
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.50    Display 5 04 (Module DSPLAY)
              IF shift in receiving part incorrect (IROF=1)
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.60    Display 3 05 (Module DSPLAY)
              Set internal status WSAF=1, ISWS=0
              Read operational crypto variable registers with contents
                              crypto variable shift registers (POCVST)
              IF reading incorrect on transmitter part (PIKGCH)
                THEN
                  Go to 2140.10.220
              ENDIF
```

```
2140.10.70          Display 5 06 (Module DSPLAY)
                    IF reading receiver part incorrect (PIKGCH)
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.80          Set internal status BSSL=1
                    Set check nibbles active
                    Set databyte STPAEH
                              Connect crypto output with input and black
                              sender clock to receiving clock (excluding
                              black interface)
                    Send STPAEH (POPAEH)
                    Display 4 26 (Module DSPLAY)
                    Reset pattern recognition circuit
                    Initiate crypto start pattern (ECCM on) (POPAEH)
                    Set data byte STTEDA
                              data readable for /u processor
                    Send STTEDA (POTEDA)
                    IF pattern recognition active
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.81          Display 4 10 (Module DSPLAY)
                    Clock Attention-word
                    Check pattern generator output during transmitting
                                                    (PIPEST)
                    IF Attention-word not transmitted
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.81A         Display * 33 (Module DSPLAY)
                    Cyclus counter =4
2140.10.81B         Read output pattern generator (PIPEST)
                    Read input reveiver mixer (PIKGCH)
                    IF not equal
                      THEN
                        Go to 2140.10.220
                    ENDIF
                    Clock 1 time
                    Decrease cyclus counter
                    IF cyclus counter not 0
                      THEN
                        Go to 2140.10.81B
                    ENDIF
2140.10.82          Display 4 15 (Module DSPLAY)
                    Check status pattern generator is busy
                    IF not active
                      THEN
                        Go to 2140.10.220
                    ENDIF
                    Display 4 20 (Module DSPLAY)
                    Transmit Attention-word till point of recognition
                    Read pattern recognition (PIPEST)
                    IF Attention-word recognised
                      THEN
                        Go to 2140.10.220
                    ENDIF
```

```
                    Display * 61 (Module DSPLAY)
                    Test RST 6.5
                    IF active
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.83          Clock one time the pattern generator
                    Read pattern recognition (PIPEST)
                    IF Attention-word not recognised
                      THEN
                        Go to 2140.10.220
                    ENDIF
                    Display * 61 (Module DSPLAY)
                    Test RST 6.5
                    IF not active
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.84          Display 4 11 (Module DSPLAY)
                    Clock untill code word Crypto-start
                    Check pattern generator output during transmitting
                          code word crypto start (PIPEST)
                    IF code word crypto start not transmitted
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.85          Display 4 21 (Module DSPLAY)
                    Clock untill recognition point crypto start
                    Read pattern generator (PIPEST)
                    IF Attention-word not recognised
                      THEN
                       Go to 2140.10.220
                    ENDIF
2140.10.86          Clock one time
                    Read pattern recognition (PIPEST)
                    IF code word crypto start not recognised
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.87          Display 4 22 (Module DSPLAY)
                    Clock till crypto
                    IF status pattern recognition initialisation
                                      incorrect
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.87A         Display 4 15 (Module DSPLAY)
                    Check status pattern generator is busy
                    IF active
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.88          Display 4 22  (Module DSPLAY)
                    Time delay 0.5 seconds
                    Clock one time
```

```
                    IF status pattern recognition and check bits
                                                        incorrect
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.89          Display 4 26 (Module DSPLAY)
                    Reset pattern recognition (POPAEH)
                    IF pattern recognition active
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.89A         Display * 61 (Module DSPLAY)
                    Test RST 6.5
                    IF active
                      THEN
                        Go to 2140.10.220
                    ENDIF
          END (DGNTST1)
```

```
DGNTST2   BEGIN (DGNTST2)
2140.10.90    Display 4 10 (Module DSPLAY)
              Read databyte STPAEH
              Force 0 to input message key register
              Clock 0 through message key register
              Preset CHANGE CRYPTO VARIABLE pattern (ECCM on)(POPAEH)
              Switch message key register as a shift around register
              Clock Attention-word
              Check pattern generator output during transmitting
                                        (PIPEST)
              IF Attention-word not transmitted
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.92    Display 4 15 (Module DSPLAY)
              Check state busy
              IF state not busy
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.95    Display 4 13 (Module DSPLAY)
              Clock untill code word CHANGE CRYPTO VARIABLE
              Check pattern generator output during transmitting
                                       code word (PIPEST)
              IF code word CHANGE CRYPTO VARIABLE not transmitted
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.96    Display 4 23 (Module DSPLAY)
              Clock untill recognition point of code word
              Read pattern recognition circuit (PIPEST)
              IF Attention-word not recognised
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.97    Clock one time (POTEDA)
              Read pattern recognition circuit(PIPEST)
              IF pattern CHANGE CRYPTO VARIABLE not recognised
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.100   Display 4 10 (Module DSPLAY)
              Clock untill end of Attention-word
              Check output pattern generator during transmitting
                                      (PIPEST)
              IF Attention-word not transmitted
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.103   Display 4 11 (Module DSPLAY)
              Clock untill code word crypto start
              Check output pattern generator during transmitting
                                (PIPEST)
              IF code word crypto start not transmitted
                THEN
                  Go to 2140.10.220
              ENDIF
```

```
2140.10.107         Display 4 22 (Module DSPLAY)
                    Clock untill code word CRYPTO START recognised
                    IF error in status Crypto pattern recognition
                              and/or checkbits
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.108         Display 4 15 (Module DSPLAY)
                    Check status busy
                    IF status busy
                      THEN
                        Go to 2140.10.220
                    ENDIF
2140.10.110         Display 4 25 (Module DSPLAY)
                    Clock untill recognition circuit is inactive
                    IF recognition circuit is active
                      THEN
                        Go to 2140.10.220
                    ENDIF
          END (DGNTST2)
```

```
DGNTST3   BEGIN (DGNTST3)
2140.10.130   Clock even number of bits till a bit is at the input of
                                                        the transmitter
2140.10.131   Force repeating code 00100111 (POTEDA)
2140.10.132   TSTCTE=32
2140.10.134   Load CTRTBA
              Display 3 30 (Module DSPLAY)
              Read output ECCM circuit transmitter part(PIKGCH)
              Load information from tabel to check
              IF output ECCM circuit transmitter part incorrect
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.136   Display 3 31 (Module DSPLAY)
              Read output mixer transmitter part (PIKGCH)
              Load information from table to check
              IF output mixer transmitter part incorrect
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.140   Display 4 32 (Module DSPLAY)
              Read output pattern generator (PIPEST)
              Load information from tabel to check
              IF output pattern generator incorrect
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.142   Display * 33 (Module DSPLAY)
              Read input mixer receiver part (PIKGCH)
              Load information from tabel to check
              IF output pattern generator incorrect
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.150   Display 5 34 (Module DSPLAY)
              Read output mixer receiver part (PIKGCH)
              Load information from table to check
              IF output mixer receiver part incorrect
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.160   Display * 35 (Module DSPLAY)
              Read output ECCM circuit receiver part (PIRDFD)
              Load information from table to check
              IF output ECCM circuit receiver part incorrect
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.161   Display 6 36 (Module DSPLAY)
              Read transmitter input red interface (PISYCO)
              Load information from table to check
              IF transmitter input red interface incorrect
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.170   Activate blocking microprocessor red data
```

```
                Display * 40 (Module DSPLAY)
                Check masks /u processor/input transmitter mixer
                IF incorrect
                  THEN
                    Go to 2140.10.220
                ENDIF
2140.10.171     Display * 41 (Module DSPLAY)
                Check masks /u processor/output receiver mixer
                IF incorrect
                  THEN
                    Go to 2140.10.220
                ENDIF
2140.10.172     Display 6 42 (Module DSPLAY)
                Check masks /u processor/red receiving data
                IF incorrect
                  THEN
                    Go to 2140.10.220
                ENDIF
2140.10.173     Display 6 43 (Module DSPLAY)
                Check masks /u processor/red transmitter data
                IF incorrect
                  THEN
                    Go to 2140.10.220
                ENDIF
2140.10.174     Deblock microprocessor red data
                Wait for ca 6 msec
2140.10.175     Decrease TSTCTE
                IF TSTCTE=0
                  THEN
                    Go to 2140.10.192
                ENDIF
2140.10.180     Load next bit from DGNINP
                Go to 2140.10.134
2140.10.192     Display 6 51 (Module DSPLAY)
                Force constant a 1 (category 1)
                Clock through
                Synchronise circuit
                Test category is 1
                IF category is not 1
                  THEN
                    Go to 2140.10.220
                ENDIF
2140.10.194     Display 6 52 (Module DSPLAY)
                Force constant a 0 (category 2)
                Clock through
                Synchronise circuit
                Test category is 2
                IF category is not 2
                  THEN
                    Go to 2140.10.220
                ENDIF
2140.10.196     Display 6 53 (Module DSPLAY)
                Force 48 times 10 (category 3)
                Clock through
                Synchronise circuit
                Test category is 3
                IF category is not 3
```

```
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.198   Display 6 51 (Module DSPLAY)
              Force constant a 1 (category 1)
              Clock through
              Synchronise circuit
              Test category is 1
              IF category is not 1
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.200   Display 6 37 (Module DSPLAY)
              Block output red data (POTEDA)
              Clock till blocking is readable
              Clock and read 3 times red data transmitter input
                                    (POSYCO)
              IF incorrect
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.202   Display 5 44 (Module DSPLAY)
              Block crypto output (POPAEH)
              Clock till blocking is readable
              Clock and read 3 times crypto output (PIPEST)
              IF incorrect
                THEN
                  Go to 2140.10.220
              ENDIF
              Release blocking
2140.10.203   Block crypto output
              Clock till blocking is readable
2140.10.203A  Clock and read 3 times crypto output (PIPEST)
              IF incorrect
                THEN
                  Go to 2140.10.220
              ENDIF
          END (DGNTST3)
```

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```
DGNTST4   BEGIN (DGNTST4)
2140.10.204   Display 4 10 (Module DSPLAY)
              Read databyte STPAEH
              Transmit compromise pattern (POPAEH and POTEDA)
              Clock Attention-word
              Check output pattern generator during transmitting
                                  (PIPEST)
              IF Attention-word not transmitted
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.205   Display 4 15 (Module DSPLAY)
              Test state busy of pattern generator
              IF not busy
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.206   Display 4 14 (Module DSPLAY)
              Check output pattern generator during transmitting
                            code word (PIPEST)
              IF compromise pattern not transmitted
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.208   Display 4 24 (Module DSPLAY)
              Clock till recognising point code word
              Read pattern recognition circuit (PIPEST)
              IF Attention-word not recognised
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.209   Clock POTEDA 1 time
              Read pattern recognition circuit (PIPEST)
              IF compromise pattern not recognised
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.210   Display 4 10 (Module DSPLAY)
              Clock Attention-word
              Check output pattern generator during transmitting
                                  (PIPEST)
              IF Attention-word not transmitted
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.212   Display 4 14 (Module DSPLAY)
              Check output pattern generator during transmitting
                                  (PIPEST)
              IF compromise pattern not transmitted
                THEN
                  Go to 2140.10.220
              ENDIF
2140.10.214   Display 4 24 (Module DSPLAY)
              Clock till recognition point code word
              Read pattern recognition circuit (PIPEST)
```

```
                IF Attention-word not recognised
                  THEN
                    Go to 2140.10.220
                ENDIF
2140.10.216     Clock one time (POTEDA)
                Read pattern recognition circuit (PIPEST)
                IF compromise pattern not recognised
                  THEN
                    Go to 2140.10.220
                ENDIF
2140.10.217     Display 4 15 (Module DSPLAY)
                Test status pattern generator busy
                IF status is not busy
                   THEN
                     Go to 2140.10.220
                ENDIF
2140.10.218     Reset pattern generator in rest mode
                Test status pattern generator is busy
                IF status is busy
                  THEN
                    Go to 2140.10.220
                ENDIF
2140.10.219     Display OK (Module DSPLAY)
2140.10.220     IF spare crypto variable present (ISAF=0)
                  THEN
                    Read spare crypto variable in crypto variable shift
                                                    register (Module VULISR)
                    IF reading error (IROF=1 and/or IRZF=1)
                      THEN
                        Set internal status ISAF=1
                    ENDIF
                 ENDIF
2140.10.222      Extinguish the leds
2140.10.230      Read front controls (Module REFRBE)
                 IF rotary function selector is in position ONDERHOUD 2
                   THEN
                     Go to 2140.10.230
                ENDIF
2140.10.240     Reset pattern generator and recognition circuit (POPAEH)
                Go to module INITSG
                Mask alarm interrupt
                Set databyte STTEDA
                          Block data to µ processor
                          data clock controlled by extern offered data
                                                    clock
                          disconnect red data input and output
                          disconnect red transmitting and receiving clock
                                      (including red interface)
                          connect transmitter data output red interface
                                    to data input ECCM circuit
                          connect sync command line to red interface
                                                          input
                          block reading received data
                          release red data output
                Wait ca 7 msec
                Release alarm interrupt
```

```
            Set databyte STSTLD
                    Fill device not selected
                    Led SYNC ALARM extinguished
                    led BEDRIJF extinguished
                    external status: Secured connection =0
                                     synchronous = 1
                                     Normal traffic = 0
            Send STSTLD (POSTLD)
            Send STTEDA (POTEDA)
            Disconnect crypto data and clock input and output
                        (excluding black interface)(POPAEH)
            Disconnect crypto data and clock input and output
                        (including black interface)(POSTBI)
            Release Attention-word interrupt
        ENDIF
2140.20 Display crypto variable settings (Module DSPSLI)
        Go to 2170 (Module FROBED)
        END (DGNTST4)
```

```
ALMTST    BEGIN (ALMTST)
2150.10   IF button ACTIVATE pressed(ACTV=1)
            THEN
              Display Blank (Module DSPLAY)
              Generate alarm interrupt (POPAEH and POTEDA)
              Delay ca 2 sec (Module DELAY)
          ENDIF
2150.20   Display crypto variable settings (Module DSPSLI)
          Go to 2170 (Module FROBED)
          END (ALMTST)
```

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```
FNCTST    BEGIN (FNCTST)
2160.10   IF button ACTIVATE is pressed (ACTV=1
            THEN
2060.10.1     Display TEST (Module DSPLAY)
              IF operational crypto variable not present (WSAF=1)
                THEN
2160.10.1.1       Mask Attention-word interrupt
                  Base key in crypto variable shift register (Module
                                                        VULISR)
                  IF reading error (IROF=1 or IRZF=1)
                    THEN
                    Set internal status TEFO=1
                    Go to 2160.10.1.100
                  ENDIF
2160.10.1.2       Load operational crypto variable register with
                       contents crypto variable shift register
                                                  (POCVST)
                  Read key generators (PIKGCH)
                  IF loading incorrect
                    THEN
                      Set internal status TEFO=1
                      Go to 2160.10.1.100
                  ENDIF
2160.10.1.3       Set internal status BSSL=1
                  Set check nibbles active
                  Set STSTLD:
                            external status: Secured connection =0
                  Send contents STSTLD (POSTLD)
                  IF spare crypto variable present (ISAF=0)
                    THEN
                      Set internal status ISAF=1
                      Check validity crypto variable (Module SLECON)
                      IF validity incorrect
                        THEN
                          Set internal status TEFO=1
                          Go to 2160.10.1.100
                      ENDIF
                      Load crypto variable shift register with
                           spare crypto variable (Module VULISR)
                      IF loading incorrect (IROF=1 or IRZF=1)
                        THEN
                          Set internal status TEFO=1
                          Go to 2160.10.1.100
                      ENDIF
                      Set internal status ISAF=0
                  ENDIF
              ENDIF
2160.10.1.10  Display TEST (Module DSPLAY)
              Lit all led's
              Set external status: synchronous inactive
              IF ECCM switch is ON
                THEN
                  Force ECMZ = 1
              ENDIF
              Energise the crypto loop relay
              Set external status: synchronous inactive
```

```
                Set STTEDA: Connect red output to red input
                            Data clock controlled by micro processor
                Send STTEDA (POTEDA)
                Time delay for 6 mseconds
                Test message key registers and alarm circuit (BRATST)
                Initiate key generator (Module INITSG)
                Mask alarm interrupt
                Set databyte STTEDA: data clock controlled by data clock
                                                controller
                Send STTEDA (POTEDA)
                Wait for ca 7 msec
                Release alarm interrupt
                IF fault (TEFO=1)
                  THEN
                    Go to 2160.10.1.100
                ENDIF
2160.10.1.20    Transmit crypto start pattern (POPAEH)
                Waitloop to synchronise (Module DELAY)
                Set external status: synchronous inactive
2160.10.1.21    Force 0 to encipher (POTEDA)
                NIVTEL=32
                Set internal status TEFO=0
2160.10.1.30    Time delay (Module DELAY)
                LEESTE=3
                IF NIVTEL is even
                  THEN
                    Output red interface transmitter has to be 0
                    Sync command has to be category 2
                    Go to 2160.10.1.50
                ENDIF
2160.10.1.40    Output red interface transmitter has to be 1
                Sync command has to be category 1
2160.10.1.50    Read output red interface transmitter (PISYCO)
                IF red interface transmitter output incorrect
                  THEN
                    Set internal status TEFO=1
                    Go to 2160.10.1.100
                ENDIF
2160.10.1.60    Read sync command (PISYCO)
                IF wrong sync category
                  THEN
                    Set internal status TEFO=1
                    Go to 2160.10.1.100
                ENDIF
2160.10.1.61    Decrease LEESTE
                IF LEESTE is not 0
                  THEN
                    Time delay (Module DELAY)
                    Go to 2160.10.1.50
                ENDIF
2160.10.1.70    Time delay 35 mseconds ((Module DELAY)
                Decrease NIVTEL
                IF NIVTEL=0
                  THEN
                    Go to 2160.10.1.100
                ENDIF
```

```
2160.10.80     IF NIVTEL is even
                 THEN
                   Force a 0
                   Go to 2160.10.1.91
               ENDIF
2160.10.1.90   Force a 1 (POTEDA)
2160.10.1.91   Go to 2160.10.1.30
2160.10.1.100  Extinguish all led's
               IF  error detected (TEF0=1)
                 THEN
                   Display **** (Module DSPLAY)
                   Display active during ca 1 second (Module DELAY)
                   Go to 2160.10.1.102
               ENDIF
2160.10.1.101  Display OK
               Display active during ca 1 second (Module DELAY)
2160.10.1.102  Read front controls (PIFRBE)
               IF rotary function selector in position TOESTEL
                 THEN
                   IF error detected (TEF0=1)
                     THEN
                       Go to 2160.10.1.102
                   ENDIF
                   Go to 2160.10.1.10
               ENDIF
2160.10.1.110  Set databyte STTEDA
                   Disconnect red data in and output
                   Connect output red data transmitter and data
                   input mixer transmitter/ ECCM
                   Disconnect sync command line from red data input
               Send STTEDA (POTEDA)
               Disconnect crypto in- and output and black transmitter
                                        and receiver clock (POSTBI)
               Set external status: synchronous active
               IF ECMZ=1 and ECMR=1
                 THEN
                   ECCM led lit
               ENDIF
           ENDIF
2160.20    Display crypto variable settings (Module DSPSLI)
           Go to 2170 (Module FROBED)
           END (FNCTST)
```

```
ALARM     BEGIN (ALARM)
10        IF in test mode (TEMO=1)
            THEN
10.1          Store PSW
              Set internal status ALTE=1
              RETURN
          ENDIF
20        Set databyte STTEDA
                       Block red data output
          Read POTEDA with STTEDA
          Set databyte STPAEH
                       Set crypto-loop and energise alarm relay
                                        (POSTBI)
           Set databyte STSTLD
                        led BEDRIJF (normal operation) lit
                        led SYNC ALARM lit
                        External status: Normal traffic = 0
                                         synchronous = 0
          Read POSTLD with STSTLD
          Set internal status INSY=0
30        Display AL (Routine DSPLAY)
          Set internal status ACTV=0
          Read front controls (Module REFRBE)
          IF Remote-zeroïze
            THEN
              Go to 40.1.1
          ENDIF
40        IF button ACTIVATE pressed(ACTV=1)
            THEN
40.1          IF rotary function selector in TRANSPORT
                THEN
40.1.1            Erase variables (Module REMZER)
                  IF erase successful (TEFO=0)
                    THEN
                      Display ZERO during ca 0.5 sec
                      Display Blank during ca 0.1 sec
40.1.2                Go to 30
                  ENDIF
              ENDIF
40.2          IF rotary function selector in ALARM RESET
                THEN
                  Go to start address.
              ENDIF
          ENDIF
50        Go to 30
          END (ALARM)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
ATTENT    BEGIN (ATTENT)
10        Store PSW
          Release alarm interrupt
          Set databyte STSTLD
                led SYNC ALARM lit
                led BEDRIJF (normal operation) extinguished
                external status: Normal traffic=0
                                 synchronous=0
          Read POSTLD with STSTLD
          Read pattern recognition (PIPEST)
          Store registers
          IF code word CHANGE CRYPTO VARIABLE recognised
            THEN
              Go to module SLWCOM
          ENDIF
15        Mask Attention-word interrupt
          Set databyte STTEDA
                       Block receive data output
          Read POTEDA with STTEDA
          Load read counter
20        IF code word CHANGE CRYPTO VARIABLE recognised
            THEN
              Go to module SLWCOM
          ENDIF
30        IF code word CRYPTO START recognised
            THEN
              Go to module CRYSTA
          ENDIF
40        IF code word COMPROMISE recognised
            THEN
              Go to module COMPRO
          ENDIF
50        Read pattern recognition (PIPEST)
          IF passive
            THEN
              Go to 60
          ENDIF
55        Decrease readcounter
          IF counter not 0
            THEN
              Go to 20
          ENDIF
60        Execute module RUST
70        Reset pattern recognition circuit
          Release Attention-word interrupt
          Reload PSW and registers
          Return to program
          END (ATTENT)
```

```
BLKDSP    BEGIN (BLKDSP)
010       Load BLKDEL1
          Load BLKDEL2
          Return to program
          END (BLKDSP)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
BRATST    BEGIN (BRATST)
10        Store registers
          Mask interrupts
          Reset alarm interrupt
          Mask Attention-word interrupt
          Block alarm circuit
          Input message key register under control of
               /u processor (POPAEH) and clock one time
20        Clock 1001 in one and 1100 in the other message key
                    register (POTEDA)
30        Clock 124 bits from random memory (RDBGAD) into both
                              message key registers (POTEDA)
40        Load random nibble
          Get 2 times a new random bit
          Clock message key registers one time (POTEDA)
          Set internal status TEMO=1, TEFO=0
          Reset alarm circuit (POPAEH)
          Set internal status ALTE=0
          Release alarm interrupt (POPAEH)
          Get new random bit
          Clock message key registers one time (POTEDA)
          IF alarm interrupt (ALTE=1)
            THEN
              Set internal status TEFO=1
          ENDIF
50        Get new random bit
          Clock message key registers one time (POTEDA)
          IF no alarm interrupt (ALTE=0)
            THEN
              Set internal status TEFO=1
          ENDIF
60        Reset alarm circuit
          Set internal status ALTE=0
          Release alarm interrupt
          Get new random bit
          Clock message key registers one time (POTEDA)
          IF alarm interrupt (ALTE=1)
            THEN
              Set internal status TEFO=1
          ENDIF
70        Increase address random memory
          Load new random nibble
          Get new random bit
          Clock message key registers one time (POTEDA)
          IF no alarm interrupt (ALTE=0)
            THEN
              Set internal status TEFO=1
          ENDIF
80        Reset alarm circuit
          Switch message key register as a shift around register
          Set internal status ALTE=0
          Release alarm interrupt
81        Clock message key registers 128 times (POTEDA)
82        IF alarm interrupt (ALTE=1)
            THEN
82.1          Set internal status TEFO=1
          ENDIF
```

100 Reset alarm circuit (POPAEH)
Set internal status (TEMO=0)
Load registers
Mask interrupts
Return to program
END (BRATST)

```
CHPG      BEGIN (CHPG
10        Load counter
          Reset register
20        Read and store output
          Clock pattern generator
          Decrease counter
          IF counter not 0
            THEN
              Go to 20
          ENDIF
30        Return to program
          END (CHPG)
```

```
CLRAIN    BEGIN (CLRAIN)
          Read POPAEH with contents register A
          Read STPAEH with contents register A
          Read new clock pulse in DO
          Read POTEDA with DO
          Return to program
          END (CLRAIN)
```

```
CLRDIN    BEGIN (CLRDIN)
          Initiate message key register (POPAEH)
          Clock message key register one time (POTEDA)
          Return to program
          END (CLRDIN)
```

```
CODE      BEGIN (CODE)
10        Preset code to pattern generator
          Clock strobe active
          Clock strobe inactive
          Return to program
          END (CODE)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

COMPRO **BEGIN** (COMPRO)
40.10 Read databyte STPAEH
Reset pattern recognition circuit (POPAEH)
Set internal status COPA=1, INSY=0
Go to module ATTENT address 60.
END (COMPRO)

CPUTST **BEGIN** (CPUTST)
Test flags (Z, S, P and CY) and (conditional) jumps
Test instruction decoder
Test registers B, C, D, E, H and L
Test register M
Test ROM
Test data bus
Test RAM
Operational memory
END (CPUTST)

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
CRYSTA    BEGIN (CRYSTA)
10        Read 6 times pattern recognition (PIPEST),
          repetition time 17,5 /usec
          IF  pattern recognition in crypto mode (mode 3)
            THEN
              Go to 20.20
          ENDIF
20.10     Load read counter
20.15     Read pattern recognition (PIPEST)
          IF pattern recognition not in crypto mode (mode 3)
            THEN
              Decrease read counter
              IF  read counter not 0
                THEN
                  Go to 20.15
              ENDIF
              Go to 20.90
          ENDIF
20.20     Set internal status ECMR=1
          IF on contrary post ECCM switch is off
            THEN
              Set internal status ECMR=0
              Set databyte STSTLD
                           Extinguish led ECCM
          ENDIF
20.30     IF ECCM swtich is on and ECCM switch contrary post is on
                                                 (ECMZ=1, ECMR=1)
            THEN
              Set databyte STSTLD
                           led ECCM lit
          ENDIF
20.50     IF recognised pattern from Mucolex II
            THEN
              IF received message key incorrect
                THEN
                  Go to 20.90
              ENDIF
          ENDIF
20.70     Set internal status CSPA=1
20.90     Set mode in not synchronous mode (INSY=0)
          Go to module ATTENT address 60
          END (CRYSTA)
```

```
DELAY     BEGIN (DELAY)
10        Store registers
20        Adjust kernel counter
30        Decrease kernel counter
          IF kernel counter is not 0
            THEN
              Go to 30
          ENDIF
40        Decrease timing counter
          IF timing counter is not 0
            THEN
              Go to 20
          ENDIF
60        Reload registers
          Return to program
          END (DELAY)
```

```
DSPLAY    BEGIN (DSPLAY)
10        Store registers
          IF new offset is different of previous offset
            THEN
10.1          Mask interrupts
              Load new offset in DSPOFS
              Calculate new start address (DSPTBA + DSPOFS - 1)
              BYTE=5
10.2          Send contents of table address to display (PODISP)
              Increase table address
              Decrease BYTE
              IF BYTE not 0
                THEN
                  Go to 10.2
              ENDIF
          ENDIF
20        Release interrupts
          Reload registers
          Return to program
          END (DSPLAY)
```

```
DSPSLI    BEGIN (DSPSLI)
10        Store registers
          IF compromise pattern recognised (COPA=1)
            THEN
              Determine offset display message COMP
              Go to 50
          ENDIF
20        IF base key present (BSSL=1)
            THEN
              IF spare crypto variable present (ISAF=0)
                THEN
                  Determine offset display message SL+B
                  Go to 50
              ENDIF
              Determine offset display message B SL
              Go to 50
          ENDIF
30        IF spare crypto variable present (ISAF=0)
            THEN
               IF operational crypto variable present (WSAF=0)
                 THEN
                   IF spare and operational crypto variables are equal
                                                        (ISWS=1)
                     THEN
                       Determine offset display message SL W
                       Go to 50
                   ENDIF
                   IF called by module NORVER (NOVE=1)
                     THEN
                       Determine offset display message blank
                       Go to 50
                   ENDIF
                   Determine offset display message R+SL
                   Go to 50
              ENDIF
              Determine offset display message SL L
              Go to 50
          ENDIF
40        Determine offset display message ZERO
50        Set display message in display (Module DSPLAY)
          Set internal status NOVE=0
          Reload registers
          Return to program
          END (DSPSLI)
```

```
KLOK      BEGIN (KLOK)
10        Load status POTEDA (STTEDA)
20        Clock data circuit
          Decrease counter
          IF counter not 0
            THEN
              Go to 20
          ENDIF
30        Return to program
          END (KLOK)



INDDEL    BEGIN (INDDEL)
          Adjust 200 mseconds
          Time delay (Module DELAY)
          Return to program
          END (INDDEL)



INITSG    BEGIN (INITSG)
10        Set code Crypto Start
          Clock code in pattern generator (Module CODE)
          Clock 8 times (Module KLOK)
20        Force address random nibble
          Increase random nibble address with 1
          Clock nibble into message key register
          Shift random nibble one time clockwise (Module KLOK)
          IF random nibble address unequal random nibble end address
            THEN
              Go to 20
          ENDIF
          Connect message key register as a shift around register
          Clock 1 time (Module KLOK)
          Set internal state RNDM = 0
          Return to program
          END (INITSG)
```

```
RDRNDB    BEGIN (RDRNDB)
100       IF random memory not active
             THEN
               IF operational crypto variable present
                 THEN
                   IF a pattern is not transmitted by the pattern
                                                 generator
                     THEN
                       Read and store random bit in random memory
                                                       (RDADRS)
                       Increase bit counter RDBITE
                       IF RDBITE more than 3
                         THEN
                           Force RDBITE to 0
                           Increase RDADRS
                           IF RDADRS equal or more RDENAD
                             THEN
                               RDADRS = RDBGAD
                               Set internal status RDNM=1
                           ENDIF
                       ENDIF
                   ENDIF
               ENDIF
          ENDIF
          Return to program
          END (RDRNDB)
```

```
REFRBE    BEGIN (REFRBE)
100       Store registers
110       Read front controls (PIFRBE)
          IF not the same as previous situation
             THEN
110.1          Renew contents
               Anti rumble delay (Module DELAY)
               Read front controls (Module PIFRBE)
               IF not the same as previous situation
                 THEN
                    Go to 110.1
               ENDIF
110.2          IF button ACTIVATE is pressed
                 THEN
                   IF the button ACTIVATE was not pressed (ACTT=0)
                     THEN
                        Set internal status ACTV=1
                   ENDIF
               ENDIF
          ENDIF
120       IF button ACTIVATE was not pressed
            THEN
              Set internal status ACTT=0
          ENDIF
130       IF button ACTIVATE is pressed
            THEN
              Set internal status ACTT=1
          ENDIF
140       Reload registers
          Return to program
          END (REFRBE)
```

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NARRATIVE DESCRIPTION OF MUCOLEX - II

```
REMZER    BEGIN (REMZER)
10        Store registers
          Mask Attention-word interrupt
          Set STTEDA
                Block data outputs
          Read POTEDA with STTEDA
          Block crypto output (POPAEH)
          Set internal status INSY=0, TEF0=0
          Set databyte STSTLD:
                              led SYNC ALARM lit
                              led BEDRIJF extinguished
                              External status : synchronous =0
                                        Normal traffic =0
          Read POSTLD with STSTLD
11        Read spare crypto variable memory with all zero's (ISBGAD)
14        Check contents of spare crypto variable memory is zero
          IF contents is not 0
            THEN
              Set TEF0=1
          ENDIF
20        Read crypto variable shift register with contents spare
                            crypto variable memory (Module VULISR)
          IF reading error (IROF=1 or IRZF=1)
            THEN
              Set TEF0=1
          ENDIF
30        Change crypto variable (Module SLEWSL)
          IF change crypto variable incorrect (SWGF=1 or SWOF=1 or
                                                SWZF=1)
            THEN
              Set TEF0=1
          ENDIF
40        IF zeroïzing correct (TEF0=0)
            THEN
              Set internal status WSAF=1, ISAF=1, BSSL=0, ISWS=0
              Set check nibbles in active
              Set external status: Secured connection =0
              Read POSTLD with STSTLD
          ENDIF
50        Reload registers
          Release Attention-word interrupt
          Return to program
          END (REMZER)
```

```
RFRRND    BEGIN (RFRRND)
10        IF pattern generator does not transmit a pattern
            THEN
              Force address to begin address random memory
15            Read 8 random bits
              Add contents to old contents modulo 2
              Store contents in random memory
              IF new nibble is 00, FF or RDLAST
                THEN
                  decrease CNSSTE
                  IF CNSSTE = 0
                    THEN
                      Set internal status RNDM = 0
                      Set control nibbles = 0000
                  ENDIF
              ENDIF
              IF new nibble is unequal 00, FF or RDLAST
                THEN
                  Force CNSTE = 5
                  Store nibble in random buffer
              ENDIF
              IF address unequal end address random memory
                THEN
                  Go to 15
              ENDIF
              Internal state RNDM = 1
              Set check nibbles in 0A05
            ENDIF
            Return to program
            END (RFRRND)
```

```
RTB040    BEGIN (RTB040)
10        Reset alarm circuit (POPAEH)
          Set internal status ALTE=0
          Release alarm interrupt
          Get new random bit
          Clock message key registers one time (POTEDA)
          IF alarm interrupt (ALTE=1)
            THEN
10.1          Set internal status TEF0=1
          ENDIF
          Return to program
          END (RTB040)
```

```
RTB050    BEGIN (RTB050)
10        Get new random bit
          Clock message key registers one time (POTEDA)
          IF no alarm interrupt (ALTE=0)
            THEN
10.1          Set internal status TEF0=1
          ENDIF
          Return to program
          END (RTB050)
```

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NARRATIVE DESCRIPTION OF MUCOLEX - II

```
RUST      BEGIN (RUST)
10        IF operational crypto variable or base key loaded (WSAF=0 or
                                                        BSSL=1)
            THEN
              IF transmitter part not in a change crypto variable
                                              procedure (SLWP)
                THEN
                  Set databyte STTEDA
                                Release receiver data output
                  Read POTEDA with STTEDA
                  Set internal status INSY=1
                  Set databyte STSTLD
                                Led SYNC ALARM extinguished
                                External status: synchronous =1
                  IF synchronous status is category 3
                    THEN
                      Set databyte STSTLD
                                led SYNC ALARM lit
                  ENDIF
              ENDIF
              Send STSTLD
              Energise alarm relay
          ENDIF
20        Return to program
          END (RUST)
```

```
SLECON    BEGIN (SLECON)
10        Store registers
          Store given memory address
          Set internal status SLF0=0
          Force BYTE=30
          Force control register=00
20        Load memory byte
          Control register = control register + memory byte
          Mask crypto variable nibble
          Increase memory address
          Deccrease BYTE
          IF BYTE is not 0
            THEN
              Go to 20
          ENDIF
30        IF control register = 00H
            THEN
              Set internal status SLF0=1
              Go to 90
          ENDIF
35        Force BYTE=30
          Force control register = FF
          IF BYTE is not 0
            THEN
              Load memory byte
              Control register = Control register + memory byte
              Mask crypto variable nibble
              Increase memory address
              Decrease BYTE with 1
          ENDIF
          IF Control register = FF
            THEN
             Set internal status SLF0=1
             Go to 90
          ENDIF
40        Memory address is given address
          Force BYTE=32
          Force PARR=00H
50        Force BTTE=4
          Load memory byte and store it in SLBR
          Get a new crypto variable bit
52        Clock PARR 1 time
          Force D0 PARR as the crypto variable bit to be clocked
          IF old msb of PARR=1
            THEN
              Invert D1 of PARR
          ENDIF
54        IF new D0 of PARR=1
            THEN
              Invert D2 and D7 of PARR
          ENDIF
60        Load new parity byte in PARR
          Decrease BTTE
```

```
          IF BYTE is not 0
            THEN
              Go to 50
          ENDIF
80        IF PARR is not 00H
            THEN
              Set internal status SLF0=1
              Go to 90
          ENDIF
90        Reload registers
          Return to program
          END (SLECON)
```

```
SLEWSL    BEGIN (SLEWSL)
10        Store registers
          Set internal status SWOF=0, SWZF=0, SWGF=0, BSSL=0, WSAF=1,
                                                ISWS=0
          Change crypto variable command to key generators (POCVST)
          Read key generators (PIKGCH)
          IF reading receiver incorrect
            THEN
              Set internal status SWOF=1
          ENDIF
11        IF reading transmitter incorrect
            THEN
              Set internal status SWZF=1
          ENDIF
20        Load spare crypto variable memory start address (ISBGAD)
          Load operational crypto variable memory start address
                                                (WSBGAD)
          Force BYTE=32
30        Load byte crypto variable
          Store byte crypto variable in operational crypto variable
                                                memory
          Decrease memory addresses
          Decrease BYTE
          IF BYTE is not 0
            THEN
              Go to 30
          ENDIF
40        Load spare crypto variable memory start address (ISBGAD)
          Load operational crypto variable memory start address
                                          (WSBGAD)
          Force BYTE=32
41        Load byte crypto variable
          Compare it with corresponding operational crypto variable
                                                byte
          IF unequal
            THEN
              Set internal status SWGF=1
          ENDIF
50        Increase spare crypto variable memory address
          Increase operational crypto variable memory address
          Decrease BYTE
          IF BYTE is not 0
            THEN
              Go to 41
          ENDIF
60        IF no error (SWOF=0, SWZF=0, SWGF=0)
            THEN
              Set internal status WSAF=0, ISWS=1)
          ENDIF
70        Reload registers
          Return to program
          END (SLEWSL)
```

```
SLWCOM    BEGIN (SLWCOM)
10        Read front controls (PIFRBE)
          IF rotary function selector in position SLEUTEL WISSEL
                                        (Change crypto variable)
            THEN
              Change the crypto variables in the key generators
          ENDIF
15        Set databyte STTEDA
                        Block red data output
          Read POTEDA with STTEDA
          Mask Attention-word interrupt
          Set internal status INSY=0 and SWPA=1
20        Read pattern recognition (PIPEST)
          IF pattern recognition circuit in crypto (Mode 3)
            THEN
              Go to 40
          ENDIF
30        Load read counter
35        Read pattern recognition circuit (PIPEST)
          IF pattern recognition not in crypto (Not in mode 3)
            THEN
              Decrease read counter
              IF read counter not 0
                THEN
                  Go to 35
              ENDIF
          ENDIF
          Go to 90
40        Set internal status ECMR=1
          IF ECCM switch of contrary post is switched off
            THEN
              Set internal status ECMR=0
              Set databyte STSTLD
                           led ECCM extinguished
          ENDIF
50        IF ECCM switch in on position and on contrary post also in
                             switched on position (ECMZ=1 and ECMR=1)
            THEN
              Set databyte STSTLD
                           Led ECCM lit
          ENDIF
60        IF pattern from MUCOLEX-II
            THEN
              IF received message key incorrect
                THEN
                  Go to 80
              ENDIF
          ENDIF
70        Set internal status CSPA=1
80        IF not in SLEUTEL WISSEL procedure (SLWP=0)
            THEN
              IF rotary function selector in position SLEUTEL WISSEL
                THEN
                  IF spare crypto variable present (ISAF=0)
                    THEN
                      Change crypto variable (Module SLEWSL)
                      IF changing correct (SWGF=0,SWOF=0,SWZF=0)
```

```
                    THEN
                      Release crypto output
                      Transmit crypto start pattern (POPAEH)
                      Set databytte STSTLD
                                  External status: Secured
                                                   connection =1
                      Read POSTLD with STSTLD
                  ENDIF
              ENDIF
          ENDIF
      ENDIF
90    Go to Module ATTENT 60
      END (SLWCOM)
```

```
SYNCT     BEGIN (SYNCT)
          Store registers
          Read strap adjustment T1 (PIADBY)
          Load appropriate cycles value from table
          Read starp adjustment Tacq (PIADBY)
          Load appropriate cycles value from table
          Calculate: SYRETW (=0 cycles)
                     SYRPTW (=0.8 + Tacq cycles)
                     SYRPDR (=17 + 3.Tacq cycles)
                     SYREDR (=22 + T1 + 2.Tacq cycles)
          Reload registers
          Return to program
          END (SYNCT)
```

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```
VULISR    BEGIN (VULISR)
10        Store registers
20        Force BTTE=36
          Set internal status IROF=0 and IRZF=0
          Read check group in accumulator (33H)
30        Clock 1 time (POCVCP)
          Rotate accumulator one time clockwise
          Decrease BTTE
          IF BTTE is not 0
            THEN
              Go to 30
          ENDIF
31        Force GRTE=19
40        Force BTTE=4
          IF contents registers HL is 00 00
            THEN
              Force register A equal to base key nible and the
                                  inverted base key nible
              Go to 50
          ENDIF
41        Load crypto variable byte
          Prepare it to clock
          Invert the most significant nible and store it at the least
                                                 significant nible
          Increase memory adress
50        Clock LSB of crypto variable byte into key generator
                                                   (POCVCP)
          Rotate crypto variable byte 1 time clockwise
          Decrease BTTE
          IF BTTE is not 0
            THEN
              Go to 50
          ENDIF
60        Decrease GRTE
          IF GRTE unequal to 0
            THEN
              Go to 40
          ENDIF
61        Force GRTE=8
70        Force BTTE=4
          Force COBR=00H
          IF the contents of registers HL is 00 00
            THEN
              Force SLBR = base key nible and inverted base key
                                          nible
              Go to 80
          ENDIF
71        Load crypto variable byte
          Prepare it to clock
          Invert the most significant nible and store it at the least
                                           significant nible
          Store it in SLBR
          Increase memory address
          Force COBR=00H
80        Rotate COBR 1 time anti-clockwise
          Load checkbits from key generators and store it in COBR
                                           (PIKGCH)
```

```
          Clock LSB of SLBR in key generator (POCVCP)
          Rotate SLBR 1 time clockwise
          Decrease BTTE
          IF BTTE is unequal to 0
            THEN
              Go to 80
          ENDIF
90        Mask receiving part of COBR
          IF incorrect
            THEN
              Set internal status IROF=1
          ENDIF
91        Mask transmitting part of COBR
          IF incorrect
            THEN
              Set internal status IRZF=1
          ENDIF
100       Decrease GRTE
          IF GRTE is unequal to 0
            THEN
              Go to 70
          ENDIF
110       Load registers
          Return to program
          END (VULISR)
```

NATO CONFIDENTIAL
NARRATIVE DESCRIPTION OF MUCOLEX - II

```
ZECRST    BEGIN (ZECRST)
10        Store registers
          Set databyte STPAEH
                    Crypto start pattern and ECCM switch on
          IF ECCM switch not in position on
            THEN
              Set databyte STPAEH
                    Crypto start pattern and ECCM switch off
          ENDIF
20        Initiate pattern generator
          Transmit pattern (Module ZNDPTR)
          Mask initiation pattern generator
          Reload registers
          Return to program
          END (ZECRST)
```

```
ZNDPTR    BEGIN (ZNDPTR)
          Initiate pattern generator
          Start pattern generator
          Store transmitted information (POPAEH)
          Mask initiation pattern generator
          Reload registers
          Return to program
          END (ZNDPTR)
```