

# Microgate-C (Si-Gate CMOS)

## CLA 2000 SERIES

- Double layer metallisation
- 5 micron channel length
- Product family:
  - CLA 21XX 840 Gates
  - CLA 23XX 1400 Gates
  - CLA 25XX 2400 Gates
- 7ns max. prop delay (2 input NAND fanout of 2 with 2mm track 0-70° C 4.5-5.5V)
- 14MHz system clock rate
- 30MHz toggle rate
- Fully auto-routed

## CLA 3000 SERIES

- Double layer metallisation
- 4 micron channel length
- Product family:
  - CLA 31XX 840 Gates
  - CLA 33XX 1440 Gates
  - CLA35XX 2400 Gates
  - CLA 37XX 4200 Gates
  - CLA 39XX 6000 Gates
- 5ns max. prop delay
- 20MHz system clock rate
- 50MHz toggle rate
- Fully auto-routed

## CLA 5000 SERIES

- Double layer metallisation
- 2 micron channel length
- Product family:
  - CLA 51XX 640 Gates
  - CLA 52XX 1232 Gates
  - CLA 53XX 2016 Gates
  - CLA 54XX 3060 Gates
  - CLA 55XX 4408 Gates
  - CLA 56XX 5984 Gates
  - CLA 58XX 8064 Gates
  - CLA 59XX 10044 Gates
- 2.5ns max. prop delay
- 40MHz system clock rate
- 100MHz toggle rate
- Fully auto-routed

# Plessey Megacell™

Now there's a VLSI design system available that's perfect for solving your Application Specific Integrated Circuit (ASIC) problems. It's **PLESSEY MEGACELL** - a complete set of advanced computer-aided engineering and design tools coupled with an advanced CMOS process for implementing VLSI integrated circuits in the system design environment.

**PLESSEY MEGACELL** redefines semicustom integrated circuit design. It allows system engineers to design complex circuits with a high level of confidence of first time success in silicon - thanks to one of the best simulation facilities available in the world. This greatly reduces time to market, eliminating the many prototyping iterations that are all too common now in VLSI design.

**PLESSEY MEGACELL** is just about as close as you can get to achieving hand-crafted results short of full custom itself. System engineers can directly create their designs using the advanced layout and routing tools provided - without the aid of integrated circuit designers. So none of the system designers' application expertise is ever lost in transition, while chips of the smallest size and lowest production cost are regularly achieved.

Supporting the **PLESSEY MEGACELL** design capability is one of the most advanced CMOS processes available. It uses a 2-micron geometry capable of providing performance comparable with advanced Schottky TTL, with clock speeds to 40MHz and toggle rates of 100MHz achievable. And Plessey has established a 200,000 square foot dedicated processing facility to guarantee the manufacturing capacity required by even the most aggressive volume considerations.

**PLESSEY MEGACELL** is truly the gateway to the future - custom VLSI performance, with confidence of first time success and fast time to market. And it's going to stay that way - with Plessey's commitment to add future capabilities for high-speed ECL processes, 1 micron and submicron CMOS processes, and advanced analog capabilities.