Consumer Microcircuits Ltd

PRODUCT INFORMATION

FX204 VSB Frequency Inverter

Obsolete Product
- For Information Only -

Publication D/204/6 November 1986
Provisional Issue

Features

- *Variable Split Band
- 300-3400Hz Bandwidth
- Programmable Split Frequency
- Crystal Oscillator Stability
- Single CMOS Chip in 28-Lead Package
- Single 5 Volt Supply

Applications

- Frequency Domain Speech Scrambler
- Fixed Code Scrambler
- Rolling Code Scrambler
- For Cellular Telephones
  Mobile Radio
  Cordless Telephones

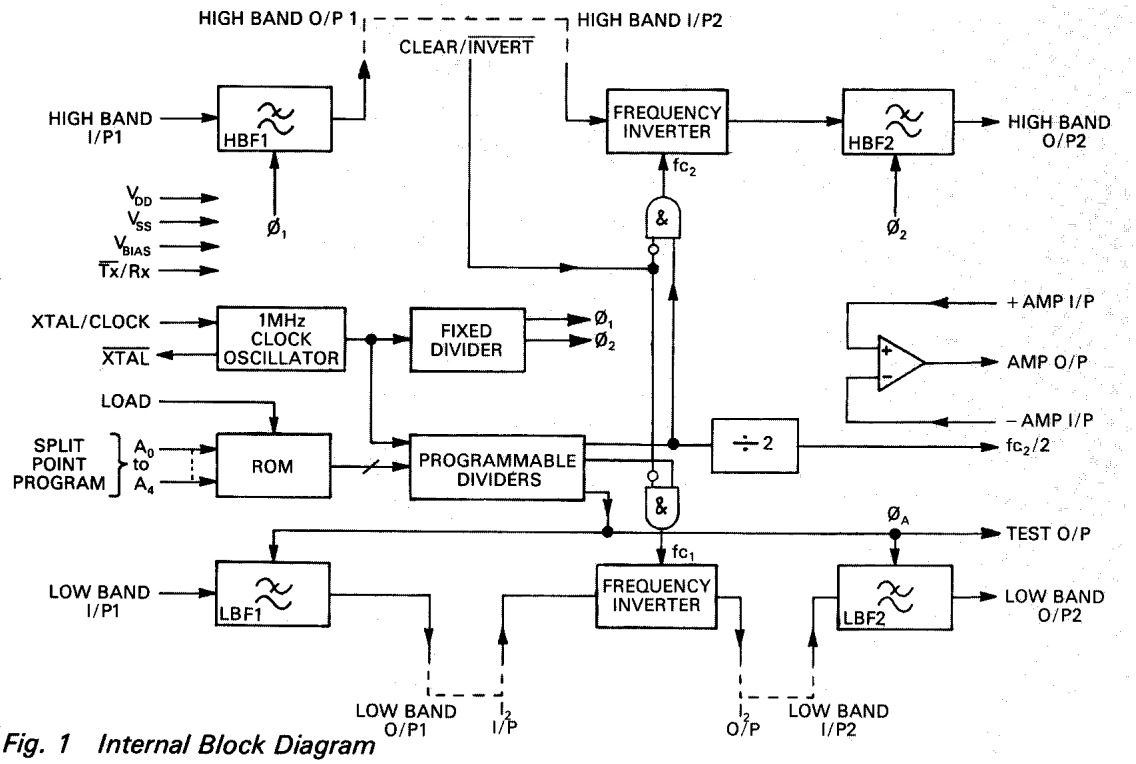


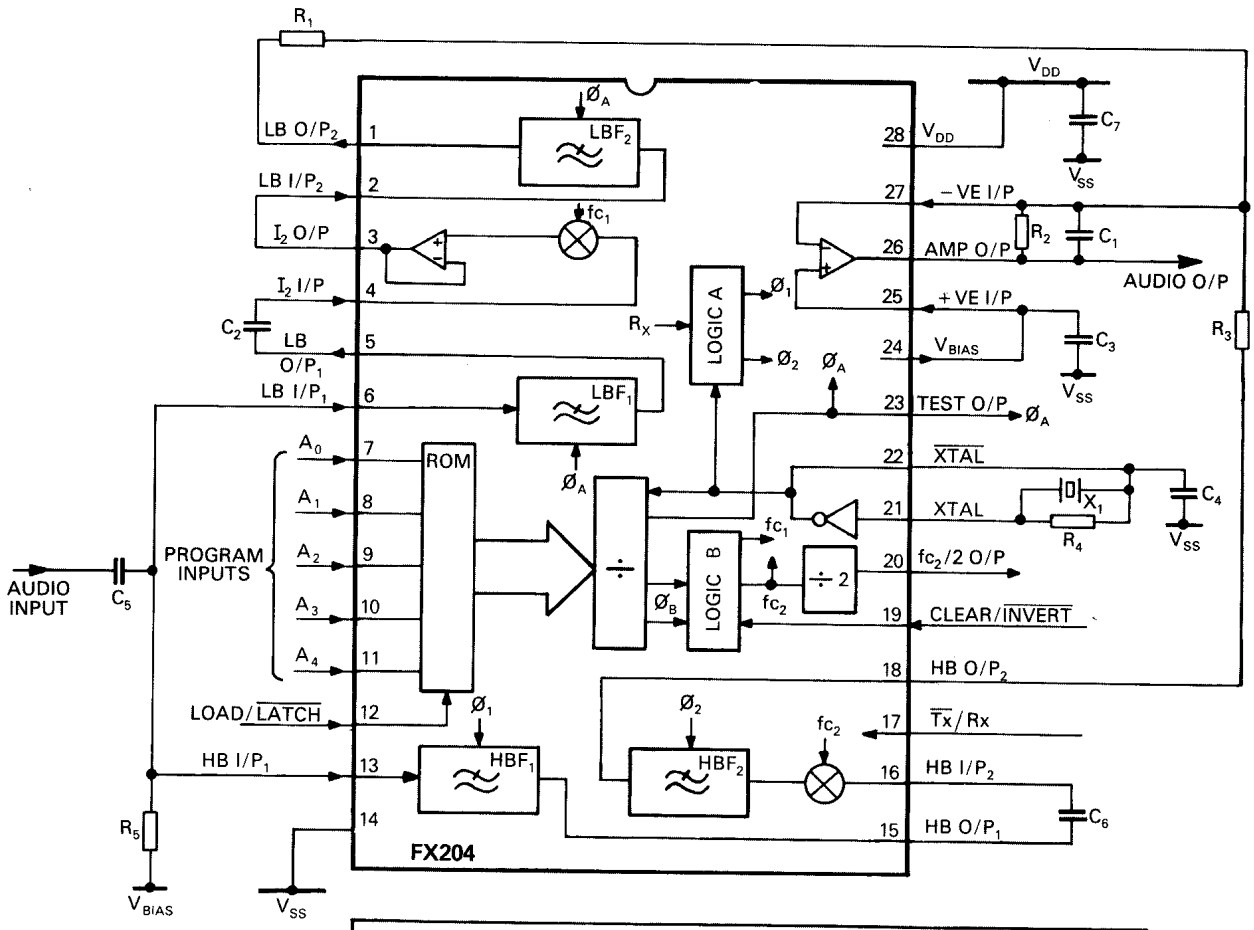
Fig. 1 Internal Block Diagram

FX204

Brief Description

The FX204 is a two-band frequency inversion device intended for use in speech scrambling applications. The FX204 uses switched capacitor filters to split the voice spectrum into high and low frequency bands and balanced modulators to invert each frequency band about its own centre frequency. The split point frequency is externally programmable to 32 different points in the range 300 to 3000Hz and makes the FX204 suitable for both fixed programmable and rolling code speech scramblers. All filter cut-off frequencies and inversion carriers are derived from a single reference crystal oscillator and facilities are provided to input and output synchronisation tones where required. Constructed in a 5 volt single supply CMOS process and available in 28-pin DIL and surface mount packages, the FX204 is suitable for use in fixed or portable equipment.

Pin Number		Function
DIL FX204J	Quad Plastic FX204LH	
1	1	**Low Band O/P 2:** This is the low band path output, normally connected to the output summing network. *(See Fig. 2.)*
2	2	**Low Band I/P 2:** Input to the low band output filter, usually directly connected to Low Band Frequency Inverter output (I_2 O/P). If not, a $V_{DD}/2$ bias should be established and signals a.c. coupled.
3	3	**I_2 O/P:** Output of the low band frequency inverter.
4	4	**I_2 I/P:** Input to the low band frequency inverter.
5	5	**Low Band O/P 1:** Output of the low band input filter, normally connected to I_2 input.
6	6	**Low Band I/P 1:** Input to the low band signal path, normally connected to the high band input and input signals a.c. coupled. *(See Fig. 2.)*
7	7	A_0
8	8	A_1
9	9	A_2
10	10	A_3
11	11	A_4
		These are the address inputs to the programming ROM for split point frequency. All inputs have pulldown resistors. *(See programming table page 5).*
12	12	**Load/$\overline{\text{Latch}}$:** This control input connects A_0_A_4 to the ROM when at logic '1', and latches current state on the negative-going edge. There is a pullup resistor to V_{DD} on this pin.
13	13	**High Band I/P 1:** Input to the high band signal path.
14	14	**V_{SS}:** Negative supply
15	15	**High Band O/P 1:** Output of the high band input filter, normally connected to High Band I/P2.
16	16	**High Band I/P 2:** Input to the high band frequency inverter.
17	17	**$\overline{\text{Transmit}}$/Receive:** This input determines the filter configuration in transmit and receive, *(See note on Principles of Operation).* There is a 1MΩ pulldown resistor to V_{SS} on this pin, which places the device in the Tx mode. An external 100kΩ pullup resistor may be used for default to Rx mode.
18	18	**High Band Output 2:** High band path output, normally connected to the output summing network. *(See Fig. 2.)*
19	19	**Clear/$\overline{\text{Invert}}$:** This input controls the operation of the inverter in both high and low band paths. When at logic 'O' the inverters are enabled. There is a pullup resistor to V_{DD} on this input. It is recommended when in 'Clear', the split point be set to 'min' or the low band O/P_2 be open circuited.
20	20	**$F_{c2}/2$ O/P:** This pin outputs the high band inverter carrier divided by 2.
21	21	**Xtal/Clock I/P:** Input to the clock oscillator inverter. 1MHz Xtal input or externally derived clock can be injected at this input.
22	22	**$\overline{\text{Xtal}}$/$\overline{\text{Clock}}$ O/P:** Output of clock oscillator inverter.
23	23	**Test O/P:** This pin outputs the sampling clock $\emptyset_A$ for the low band filters.
24	24	**V_{BIAS}:** Bias or analogue ground pin and is internally set to $V_{DD}/2$.
25	25	**+VE Amp I/P:** Non-inverting input to summing amplifier.
26	26	**Amp O/P:** Output of summing amplifier.
27	27	**−VE Amp I/P:** Inverting input to summing amplifier.
28	28	**V_{DD}:** Positive supply.



Tolerances
Resistors ± 10%
Capacitors ± 20%

Component References

Component	Unit Value	Component	Unit Value
R_1	100k	C_3	1µ
R_2	100k	C_4	33p
R_3	82k	C_5	15n
R_4	1M	C_6	1n
R_5	100k	C_7	1µ
C_1	150p	X_1	1MHz
C_2	1n		

Fig. 2. External Component Connections

The FX204 consists of parallel high and low band frequency inverters, the transition or split point frequency between these bands being varied by changing the clock signals applied to the filters and modulators, *(refer to Principles of Operation on Page 5).*

These clock signals are derived from a 1MHz crystal controlled reference oscillator via programmable dividers. The exact relationship between the split point frequency and the modulator carrier frequencies is shown in Table 2. The division ratios for each of 32 different split points are contained in an on-chip READ ONLY memory, the ROM address is externally set via 5 programming inputs and may be continuously updated or latched.

The inversion carrier signals (f_{c1} and f_{c2}) to both inverters may be inhibited by an external logic signal. Under these conditions signals are not inverted in either signal path. A summing amplifier is provided to combine the outputs of the high and low band paths. The transmit/receive logic input is used to reconfigure the cutoff frequencies of the filters in transmit and receive to optimise dynamic performance. The high band inversion carrier signal divided by two is output as a synchronisation tone source if required. In addition the sampling clock to the low band filters ($\emptyset_A$) is output as a test signal.

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	FX204J	−30°C to + 85°C
	FX204LH	−30°C to + 70°C
Storage temperature range:	FX204J	−55°C to +125°C
	FX204LH	−40°C to + 85°C

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5V, T_{amb} = 25°C, Ø = 1MHz, ΔØ = 0.

Characteristics	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply voltage V_{DD}		4.5	5.0	5.5	V
Supply current I_{DD}		—	7.5	10.0	mA
Input Logic '1'		3.5	—	—	V
Input Logic 'O'		—	—	1.5	V
Output Logic '1'		4.0	—	—	V
Output Logic 'O'		—	—	1.0	V
Dynamic Characteristics					
Signal Input Impedance		1	—	—	MΩ
Signal Output Impedance		—	—	1	kΩ
Oscillator Frequency		—	1	—	MHz
Passband Gain	1	—	0	—	dB
Passband Ripple	1, 5, 6	—	±2	—	dB
Lower 3dB point (Transmitted)	2, 4,	150	—	—	Hz
Upper 3dB Point (Transmitted)	2, 4	—	—	3430	Hz
Lower 3dB Point (Recovered)	1	—	330	—	Hz
Upper 3dB Point (Recovered)	1	—	2660	—	Hz
Output Noise	1, 3	—	−40	—	dBm
Max. Input Signal		—	+6	—	dBm
Stopband Attenuation	5	40	—	—	dB

Notes: 1. *Measured at the output of the descrambler in a scrambler-descrambler system with a transmission channel having a flat amplitude response and bandwidth of 300Hz to 3400Hz.*
2. *At output of scrambler, prior to transmission channel.*
3. *With input to scrambler ac short circuited.*
4. *Split point = 2800Hz.*
5. *Relative to mean passband gain of each filter.*
6. *Not including split point frequency ± 150Hz.*

Output Loading

Large capacitive loads could cause the output pins of this device to oscillate. If capacitive loads in excess of 200pF are unavoidable, a resistor of typically <100Ω put in series with the load should minimise this effect.

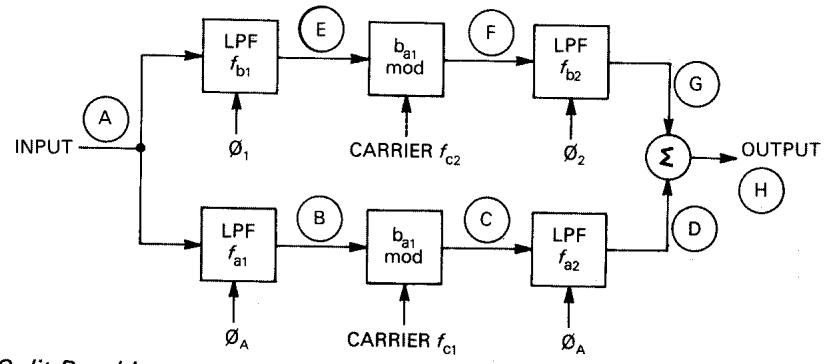
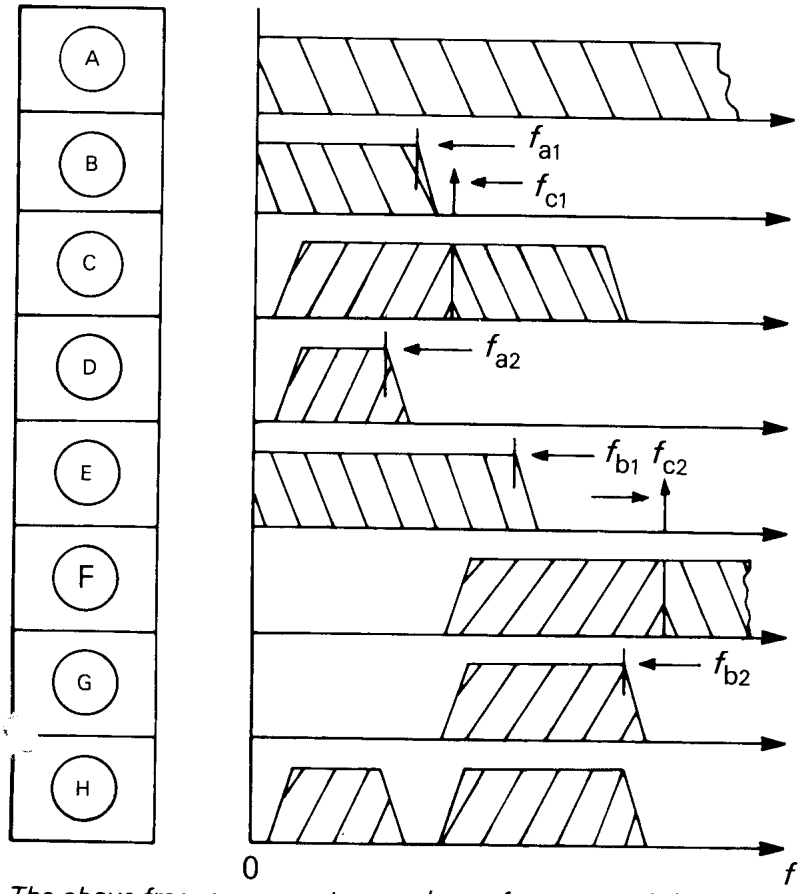


Fig. 3 Schematic of Split Band Inverter

The following table shows the frequency spectrum at each point in the above schematic diagram and describes the function of each circuit element.

Table 1 Frequency Spectrum Versus Circuit Element Functions



A	Input frequency band must be <8kHz.
B	$f_{c1} = f_{a1} + 300$Hz Input band limited by LPF at f_{a1}(split point frequency).
C	Spectrum inverted around f_{c1}, generating upper and lower sidebands.
D	Upper sideband removed by LPF at f_{a2}, $f_{a2} = 0.96\ f_{a1}$.
E	Input band limited by LPF at f_{b1}, f_{b1} is fixed at 2700Hz. $f_{c2} = f_{a1} + 3400$Hz.
F	Spectrum inverted around f_{c2}, generating upper and lower sidebands.
G	Upper sideband removed by LPF at f_{b2}, f_{b2} is fixed at 3400Hz.
H	Upper and lower bands combined in summing amplifier

The above frequency spectra are shown for a transmitting device, the filter cut-off frequencies f_{a1} and f_{b1} are reversed with f_{a2} and f_{b2} respectively when the device is receiving (de-scrambling).

Programming Table 2

ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{c1}	High Band Carrier, Hz f_{c2}	ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{c1}	High Band Carrier, Hz f_{c2}
00000	2800	3105	6172	10000	1135	1436	4504
00001	2625	2923	6024	10001	1050	1351	4424
00010	2470	2777	5813	10010	976	1278	4347
00011	2333	2631	5681	10011	913	1213	4310
00100	2210	2512	5555	10100	857	1157	4273
00101	2100	2403	5494	10101	792	1094	4166
00110	2000	2304	5376	10110	736	1037	4132
00111	1909	2212	5263	10111	688	988	4065
01000	1826	2127	5208	11000	636	936	4032
01001	1750	2049	5102	11001	591	891	3968
01010	1680	1984	5050	11010	552	853	3937
01011	1555	1858	4950	11011	512	813	3906
01100	1448	1748	4807	11100	471	772	3846
01101	1354	1655	4716	11101	428	728	3816
01110	1272	1572	4629	11110	388	688	3787
01111	1200	1501	4587	11111	350	650	3731

The principle application of the FX204 VSB Frequency Inverter is that of a frequency domain speech scrambler, the device may be used as a scrambler (transmitter) or a de-scrambler (receiver). The device requires a transmission channel of 300Hz to 3400Hz and will restrict the bandwidth of input signals between 300Hz and 2700Hz, the difference between the transmitted bandwidth and the transmission channel bandwidth is because the high band is shifted by 700Hz in transmission to separate the bands and reduce spurious outputs. The FX204 can, therefore, be used as a fixed two-band inversion scrambler with 32 codes, (relatively few codes are mutually unintelligible), or as a rolling code scrambler. The rolling code is established by changing the code (split point frequency) at several times per second resulting in a large number of usable codes. Rolling code scramblers require timing or synchronisation information to be transmitted with the scrambled speech to permit code framing to be achieved. Synchronisation is accomplished by sending an FSK data burst at the start of each transmission or by continuous outband tone signals with optional phase reversals.

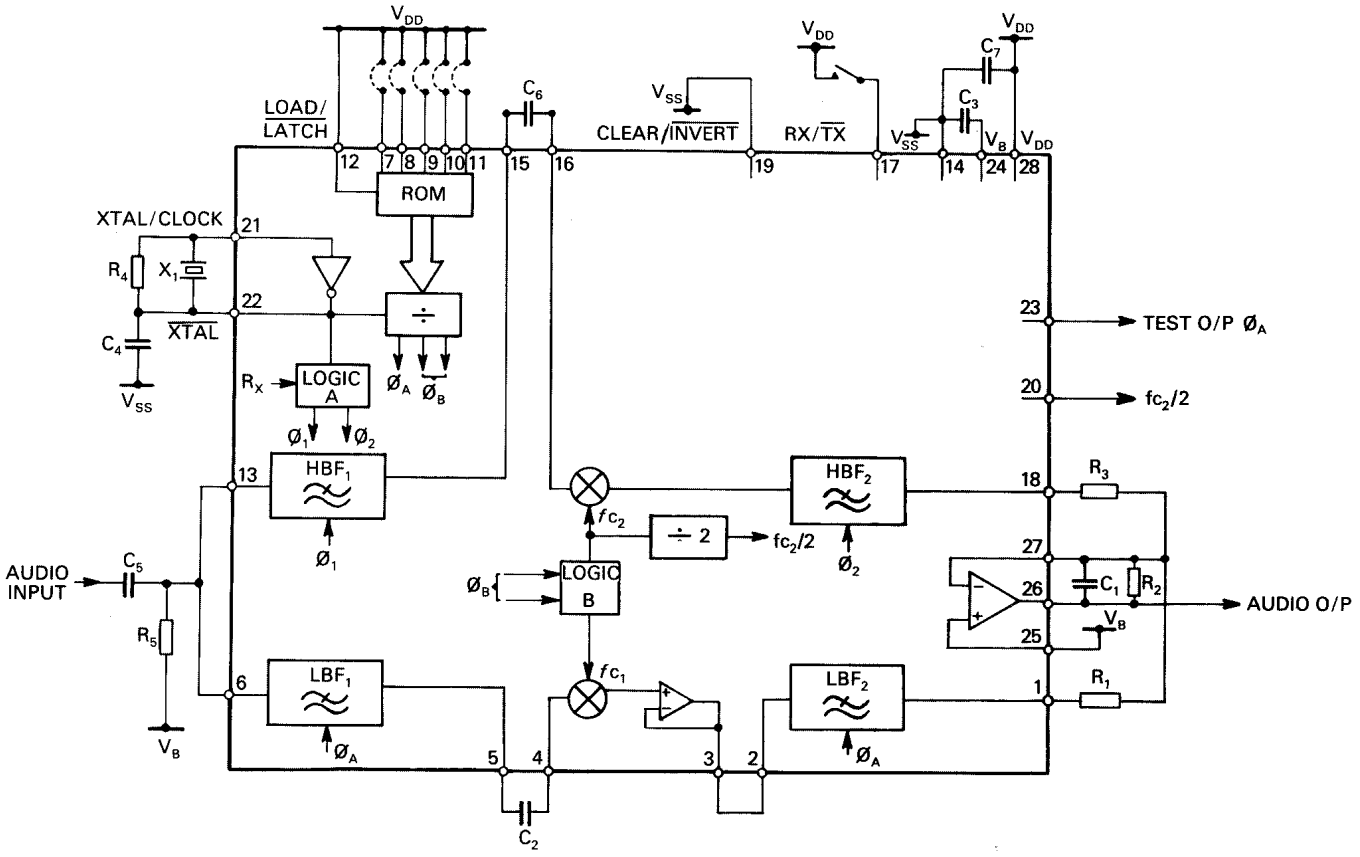


Fig 4. Application of FX204 as a fixed code scrambler

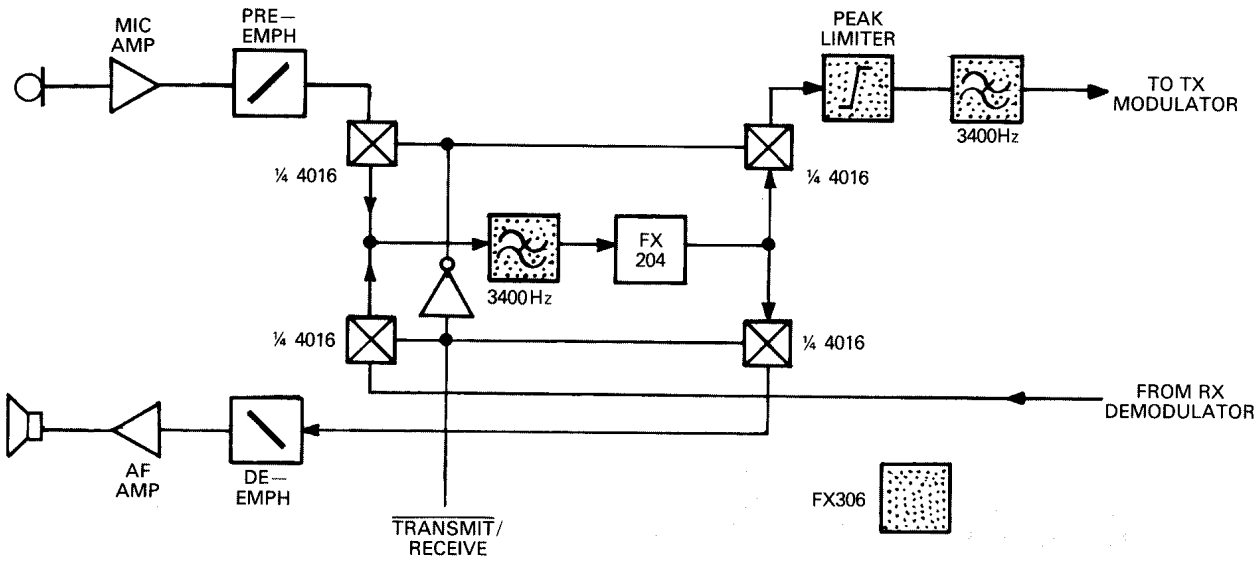


Fig 5. FX204 in PMR half duplex application

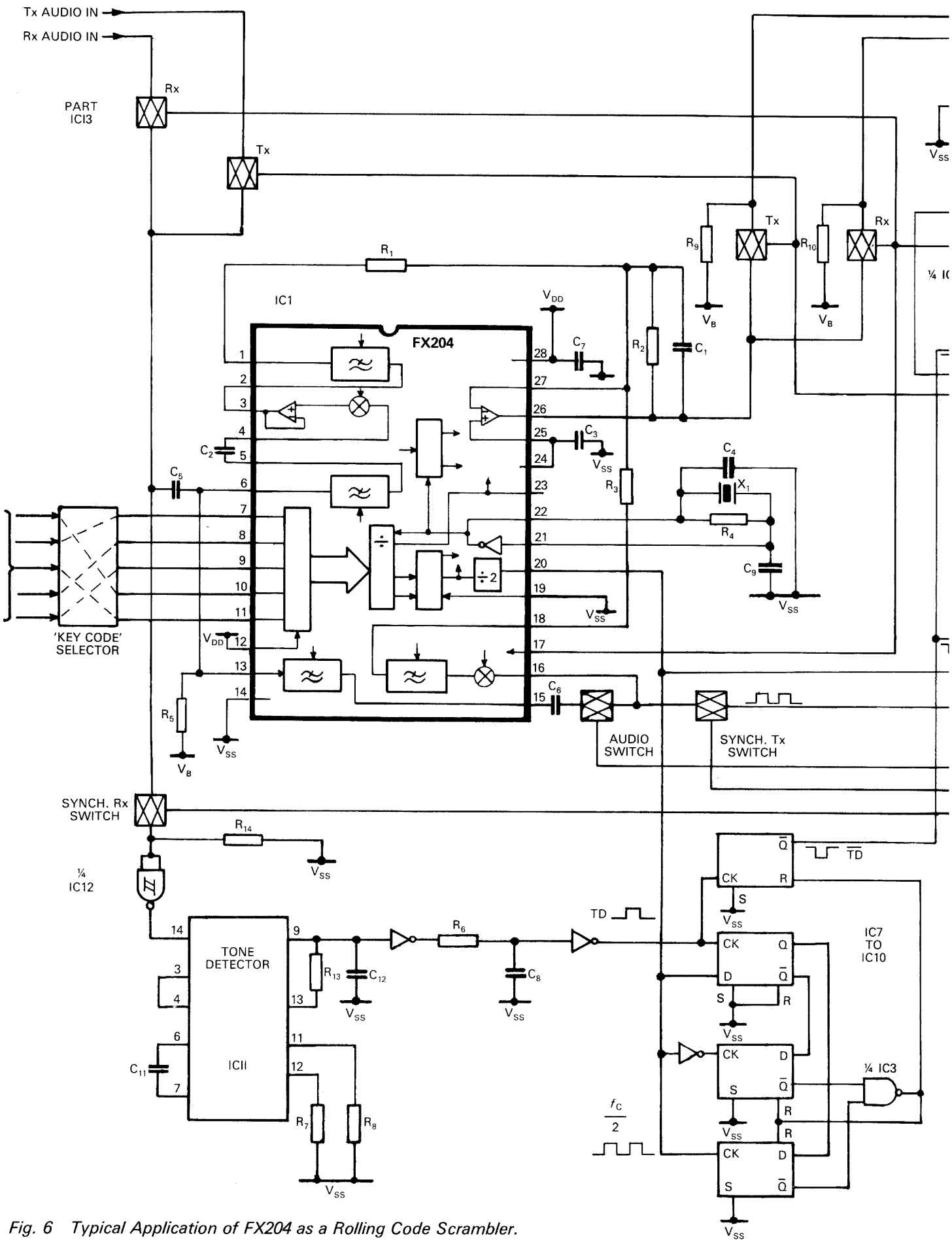
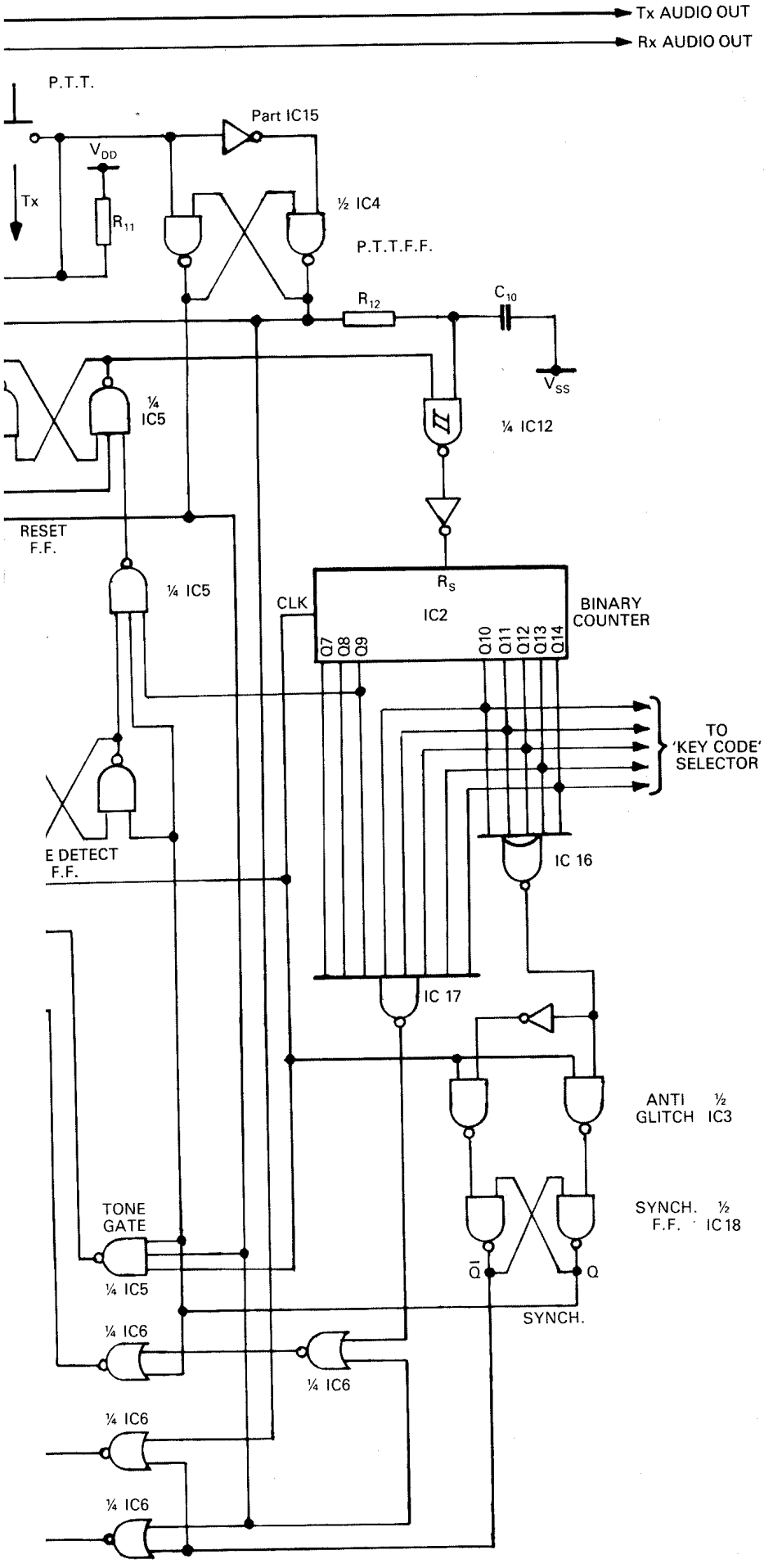


Fig. 6 Typical Application of FX204 as a Rolling Code Scrambler.
(See page 9 for description)



Component References

Component	Unit Value
R_1	100k
R_2	100k
R_3	82k
R_4	1M
R_5	100k
R_6	1M
R_7	270k
R_8	100k
R_9	1M
R_{10}	1M
R_{11}	100k
R_{12}	100k
R_{13}	100k
R_{14}	1M
C_1	150p
C_2	1n
C_3	1μ
C_4	33p
C_5	15n
C_6	1n
C_7	1μ
C_8	33n
C_9	10p
C_{10}	1n
C_{11}	4.7n
C_{12}	1n
X_1	1MHz
IC1	FX204
IC2	MC14020
IC3,IC4	MC14011
IC5	MC14023
IC6	MC14001
IC7—IC10	MC14013
IC11	MC14046
IC12	MC14093
IC13, 14	MC14016
IC15	MC14049
IC16	MC14078
IC17	MC14068
IC18	MC14011

or equivalents

Tolerances
Resistors ± 10%
Capacitors ± 20%

FX204 Rolling Code Application

Figure 6 is the circuit diagram of a rolling code scrambler using the FX204 with a selectable key code format and tone synchronisation.

System Description

The rolling code presented at the FX204 ROM consists of a 32 step, 5 bit binary code. The hop period varies with the selected high band carrier frequency (f_{c2}) and is determined by the formula; step duration $= \frac{1022}{f_{c2}}$

Synchronisation is achieved by a transmitter toneburst of $f_{c2}/2$ every 32 codes, the tone repetitions being used at the receiver to confirm continuing conversation. Using the key code selection and altering toneburst/counter relationships can ensure many private code configurations. Further receivers with the same key code configuration may join an established 'net' at the next toneburst occurrence. Receiver counter(s) will reset within one code cycle (7 secs) of the transmission ending. *(See Fig. 7.)*

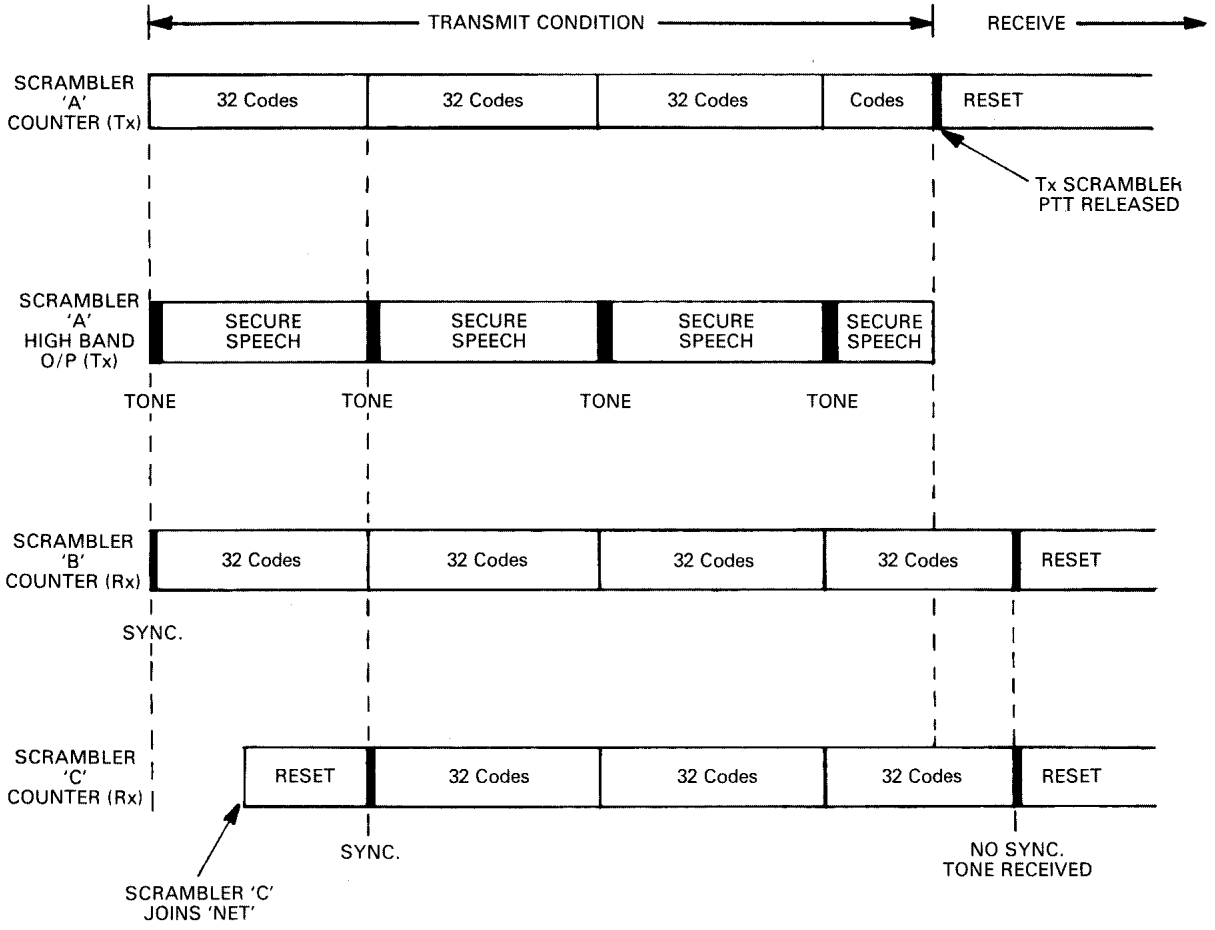


Fig. 7 Synchronisation of Counters with Scrambler 'C' joining an established 'net'.

(See Fig. 6.)

P.T.T. F.F: Controlled by the radio Push to Talk System puts the circuitry into Transmit or Receive.

Binary Counter: Provides the 5 bit, 32 step rolling code for the FX204 ROM address, and overall circuit timing. This counter is clocked by half carrier frequency of the selected high band carrier. *(See Table 2.)*

Key Code Selector: A switch or 'patch' panel to alter code sequence even further. Both Receive and Transmit stations must be set the same.

SYNCH. F.F: The Q output of this element (SYNCH) is a logic 1 when the counter state is all low, the chosen start code of the 32 code sequence.

SYNCH. Tx Switch: Used to switch one code period of tone frequency ($f_{c2}/2$) for transmitter toneburst.

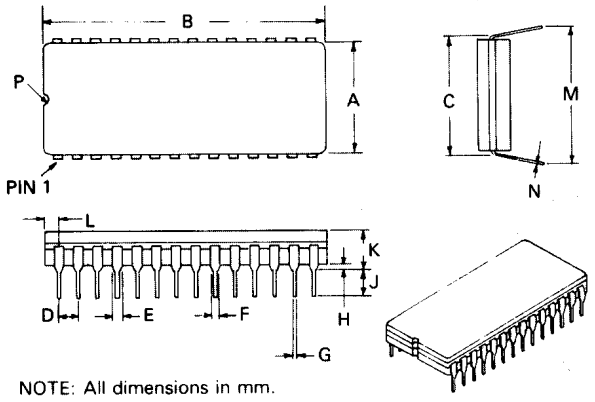
AUDIO Switch: This switch opens both Rx and Tx high band audio lines during the tone period to prevent annoying tone on audio.

D TYPE F.F's: These devices provide a clean negative pulse from a detected tone.

TONE DETECTOR: This is a PLL element arranged to detect tones higher than 2400Hz ($f_{c2}/2$ tone = 3086Hz).

RESET F.F: This element will reset the Binary counter if a tone has not been received by halfway through the first code step.

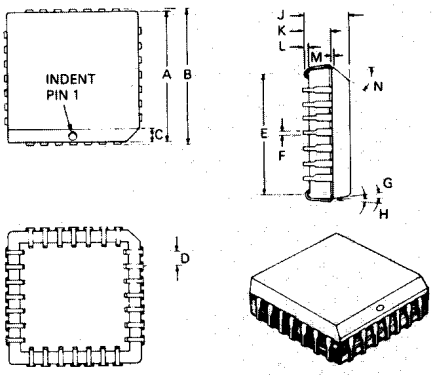
The FX204J, the cerdip package, is illustrated in *Figure 8.* The 'LH' version is shown in *Figure 9.* The 'LH' package is supplied in a conductive tray for handling convenience. The FX204LH package has an indent spot adjacent to Pin 1 and a chamfered corner between Pins 4 and 5 to allow complete identification. Pins number anti-clockwise when viewed from the top (indent side).



NOTE: All dimensions in mm.

DIMENSION	MAX	MIN	DIMENSION	MAX	MIN
A	13.36	13.06	H	1.30	0.50
B	37.05	36.58	J	3.81	3.00
C	15.7	15.5	K	5.57	4.49
D	Typical	2.54	L	2.54	–
E	Typical	1.39	M	Typical	17.00
F	Typical	0.81	N	Typical	0.25
G	Typical	0.45	P	Typical	0.64

The FX204J/LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX	MIN
A	11.6	11.4
B	12.6	12.3
C	1.1 x 45°	TYPICAL
D	1.3	TYPICAL
E	10.8	10.0
F	0.46	TYPICAL
G	7°	3°
H	7°	3°
J	4.5	4.3
K	2.5	TYPICAL
L	1.1	0.5
M	0.59	TYPICAL
N	45°	TYPICAL

FX204J **28-pin cerdip DIL**
FX204LH **28-lead plastic leaded chip carrier.**